

High-Performance SiC Power Module Development

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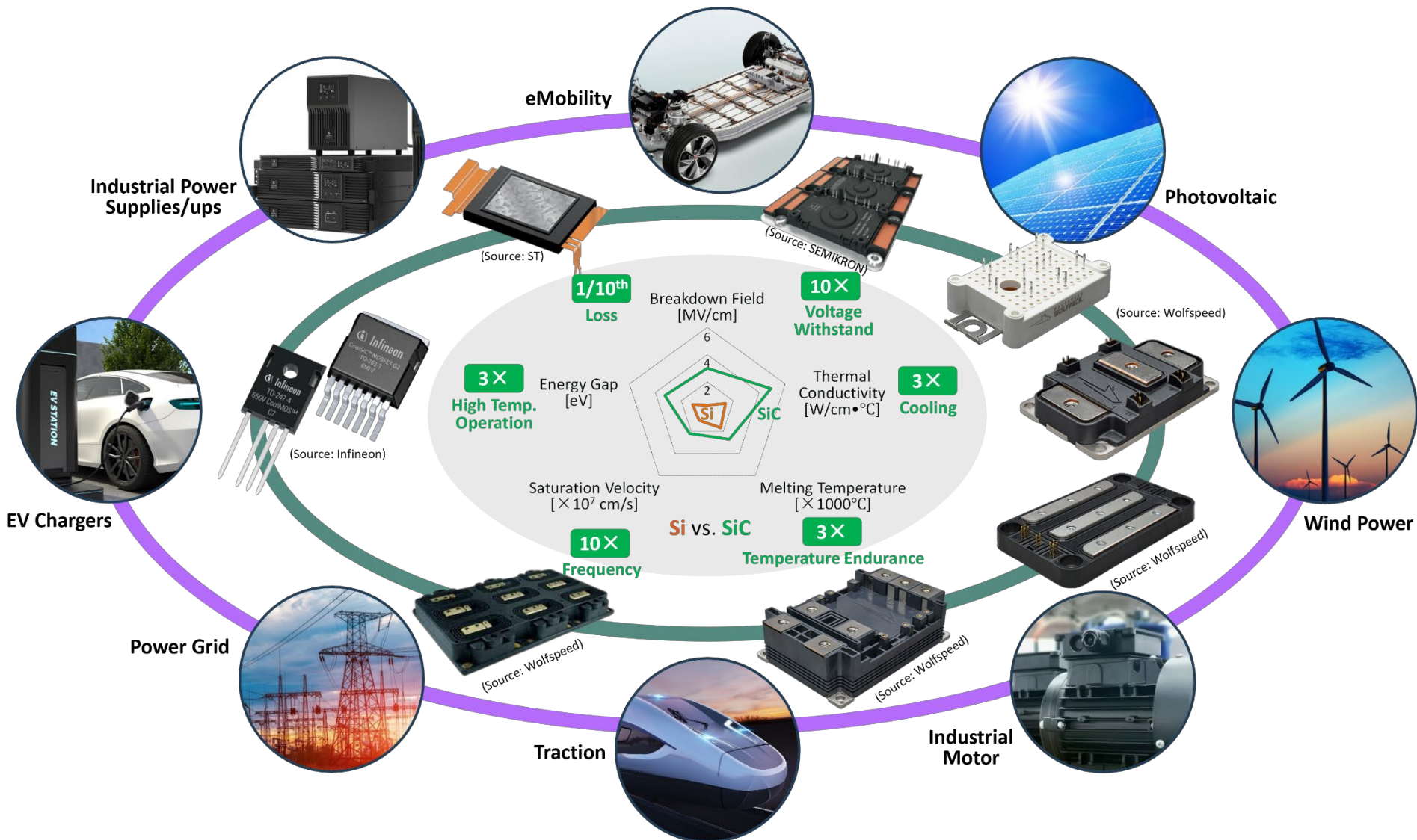
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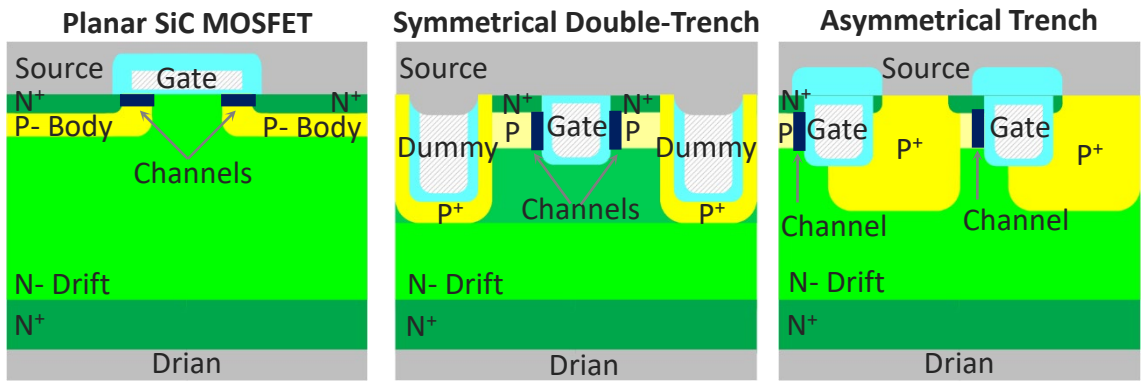
Silicon Carbide Power Device: Opportunities



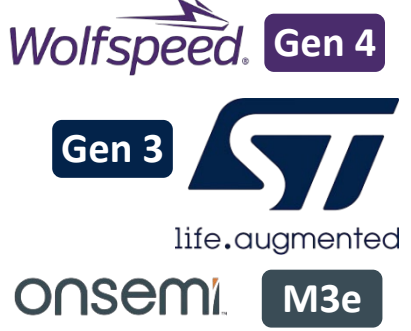
* Power SiC device market is forecast to grow nearly to \$9B with continuing penetration of SiC in automotive, along with industrial applications. (Source: Power SiC 2023, YOLE)

More efficient, smaller, and lighter than Si-Based System

Silicon Carbide Power Device: Challenges



3.3 kV SiC devices become a commercial reality



SiC Device Technologies (Rapidly evolving)

Automotive Modules

- DSC
- SSC + Pin fin
- Epoxy molding

SiC Power Module Packaging



Challenges on Module Packaging

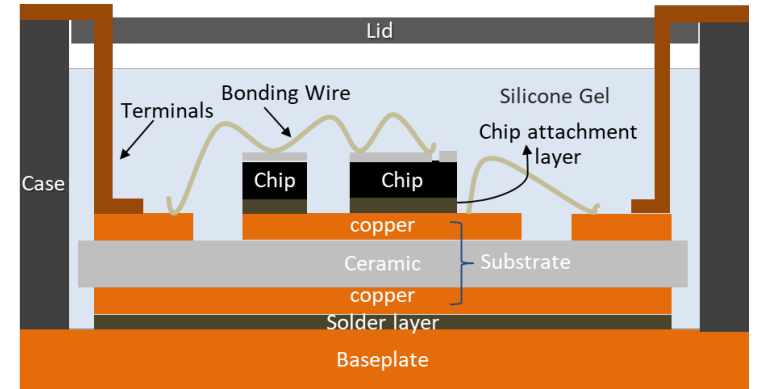
<p>High-thermal dissipation structures:</p> <ul style="list-style-type: none"> Structured baseplate Baseplate-free structure Double-sided cooling 	<p>High temp. & reliable materials:</p> <ul style="list-style-type: none"> AlN & Si3N4 Substrates Silver & copper sintering Copper wire bonding High-temp epoxy & silicone gel
<p>High insulation structure & EMI reduction/optimization design:</p> <ul style="list-style-type: none"> Stacked substrates with patterned middle layer copper 	<p>Low-inductance structures & interconnections:</p> <ul style="list-style-type: none"> wire bondless techniques (clip, metal spacer, lead frame.....)

SiC chips:

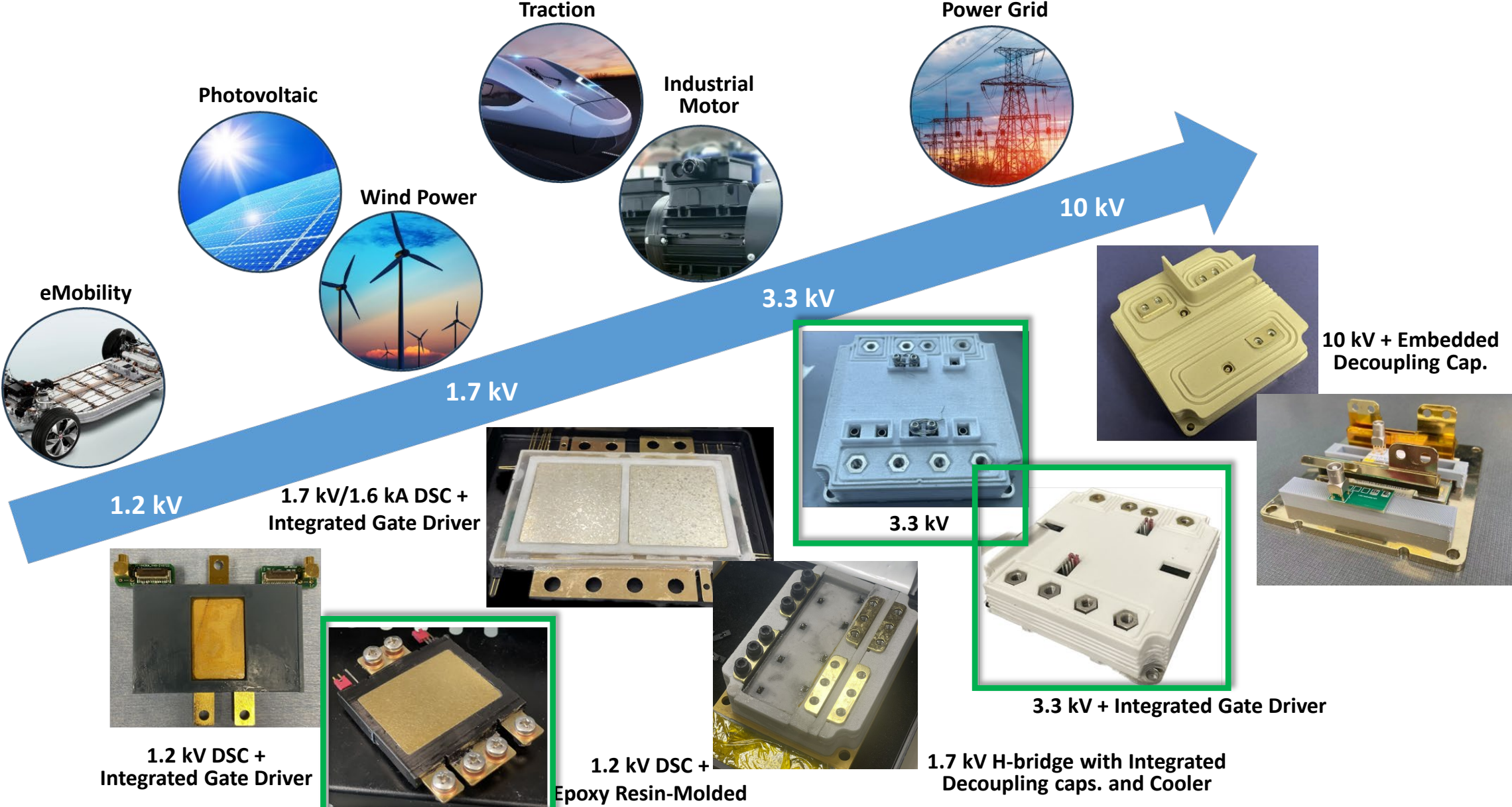
- High Temp
- Fast Switching
- High Voltage

More Effort Needed

Current (most available): Standard or enhanced Module Packaging based on Traditional Structure

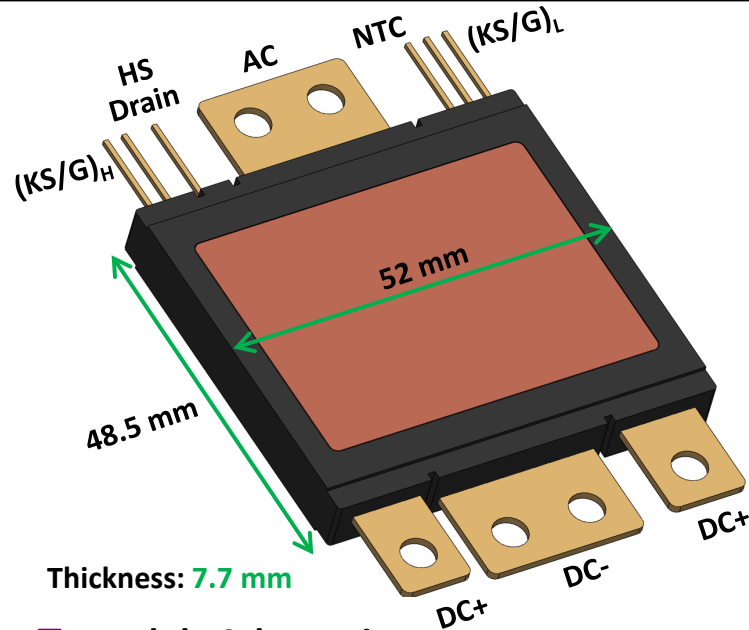


UA's Module Progression

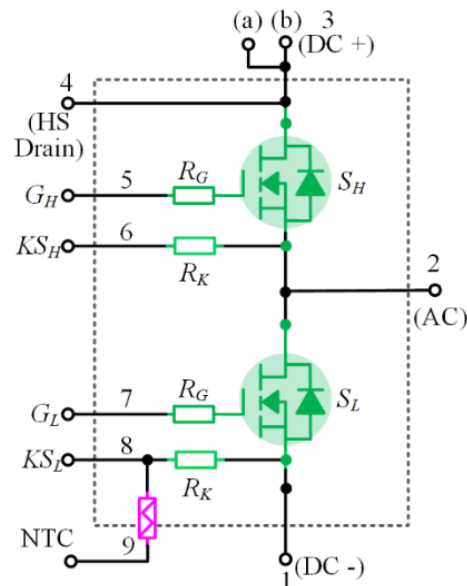


1.2 kV Double-sided cooled (DSC) SiC-based Half-Bridge Module Development

Module Specifications & Features



Module Schematic



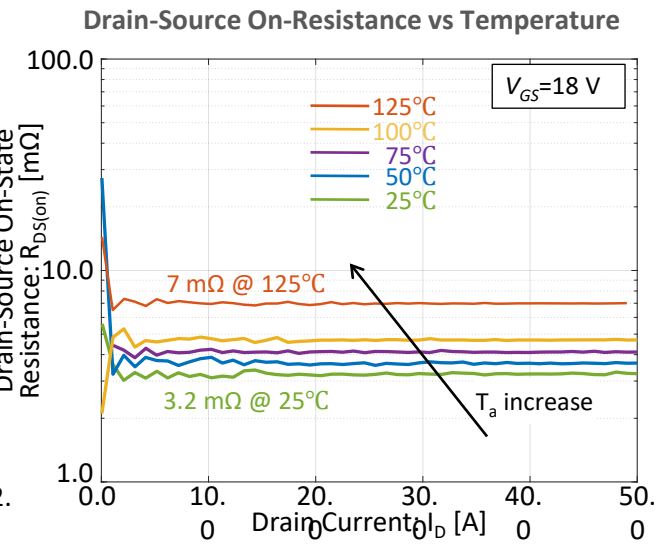
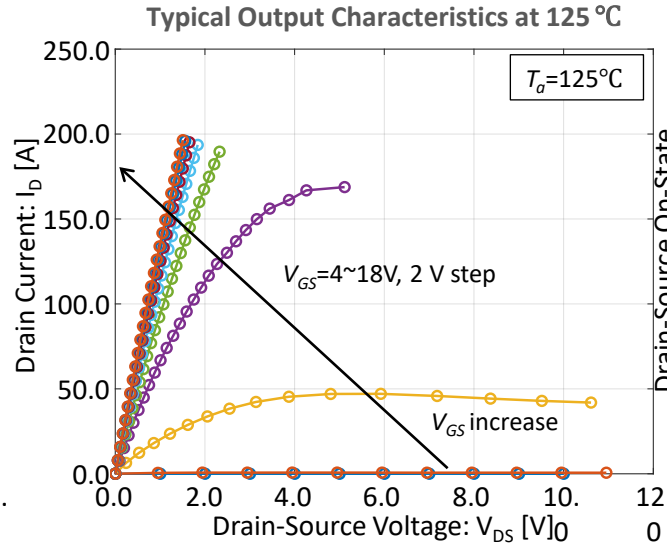
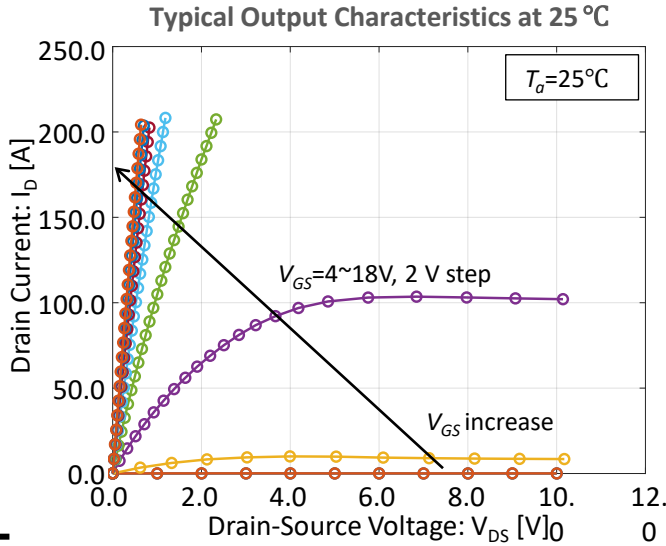
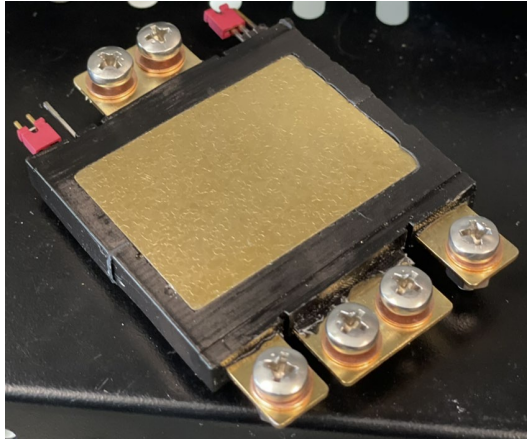
Main Specifications

Rating		1.2 kV/400 A (@ $T_c = 25^\circ\text{C}$) (DC)
Configuration		Half-Bridge Module
Dimensions		52 × 48.5 × 7.7 (mm) (= 19.4 cm ³)
Clearance & Creepage distances	Between terminals	Mini. 3 mm and 4 mm
	To grounded heatsink	Mini. 7.5 mm and 7.5 mm

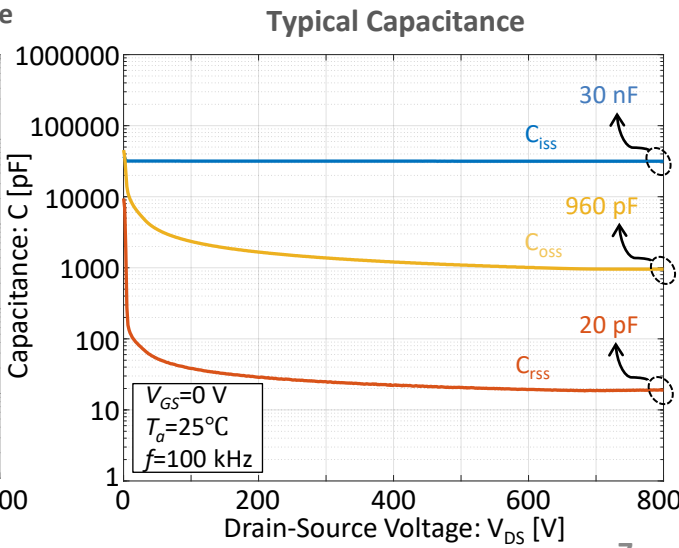
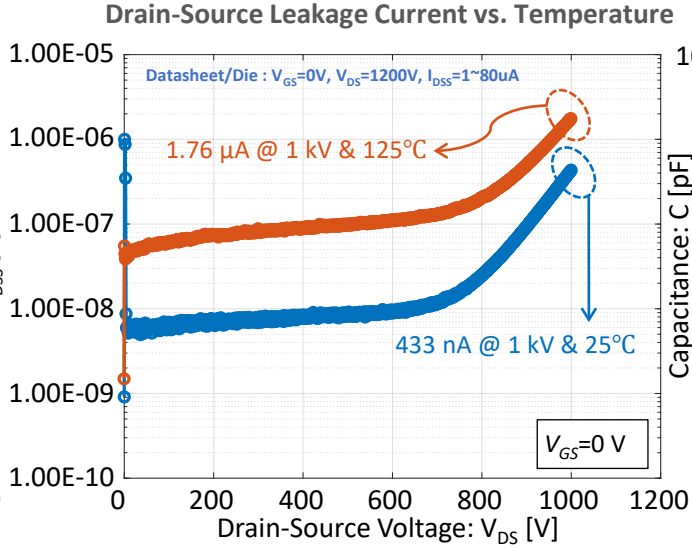
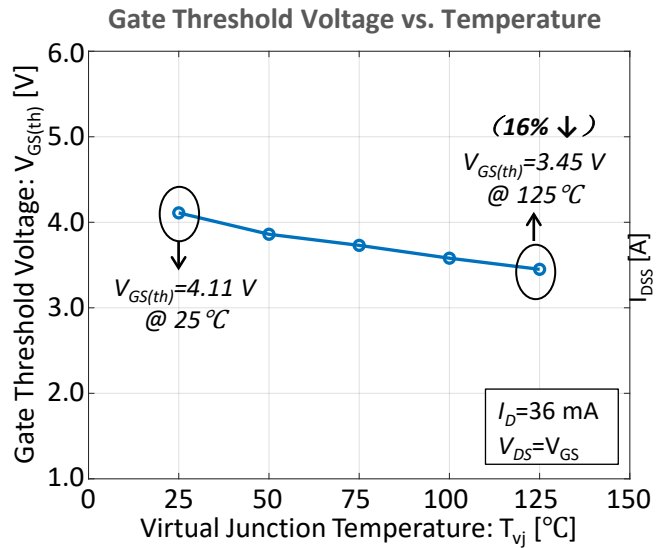
Technical Features

- **Full SiC MOSFET Module**, 4 die per switch position
- **Cu-Mo metal spacers** for chip topside power connections and **compact sandwich structure** enable low commutation-loop inductance design (Estimated **2.53 nH @ 10 MHz**)
- **Double-sided cooled structure** to achieve better thermal performance
- Combination of SiC device + **Si₃N₄ AMB Substrate** (good CTE matching) for high reliability
- **Molding process using epoxy resin** as encapsulant to deliver high reliability and high mechanical robustness
- **Integrated gate & Kelvin source resistors** to reduce high peak currents that may flow in gate loop as well as help to improve dynamic sharing in gate loop
- **Embedded temperature sensing** enables system-level temperature protection

Typical Static Characteristics of Modules



Drain-source voltage @25°C	1200 V	
Gate threshold voltage @25°C	4.1 V~4.2 V @ $I_D=36\text{ mA}$	
Drain-source on-state resistance @25°C	3 mΩ~5 mΩ	
Drain-source leakage current @25°C	<1 uA @ $V_{DS}=1\text{ kV}$	
Input capacitance	30 nF	$V_{GS}=0\text{ V}$ $V_{DC}=800\text{ V}$ $f=100\text{ kHz}$ $V_{AC}=25\text{ mV}$
Output capacitance	960 pF	
Reverse transfer capacitance	20 pF	

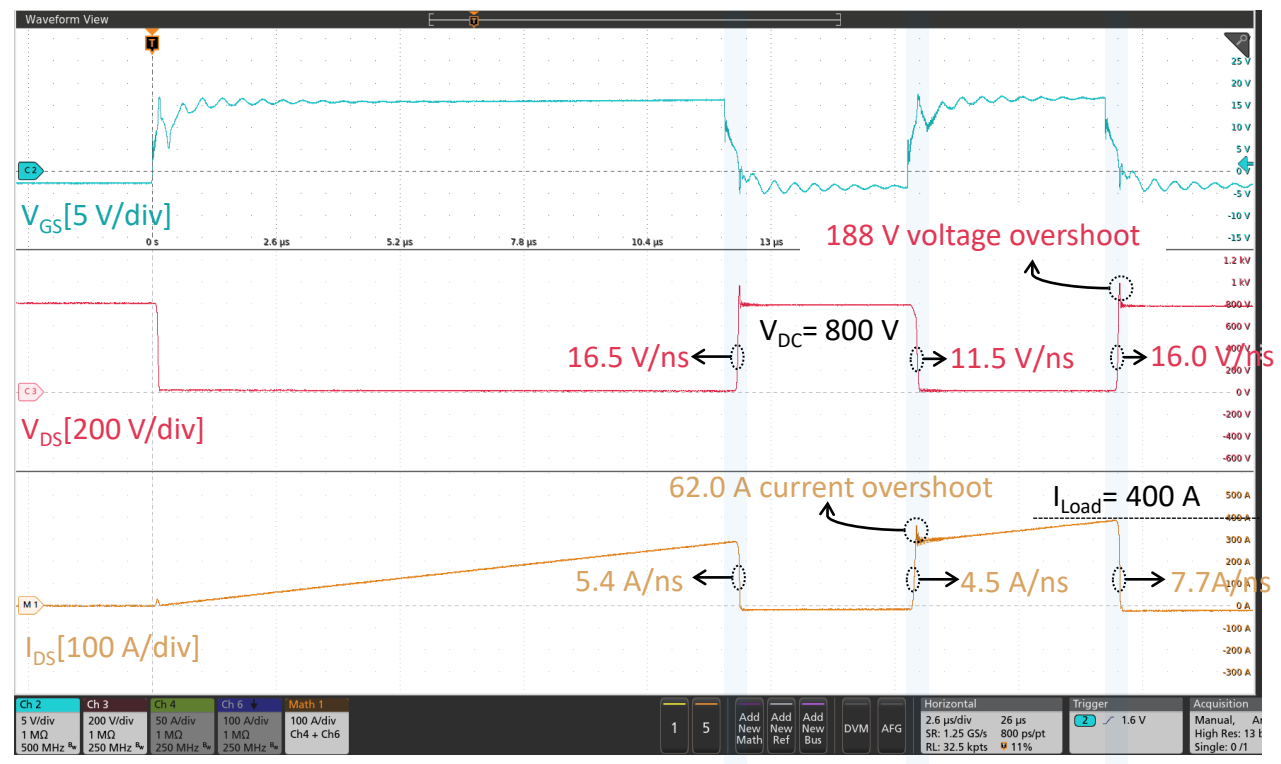
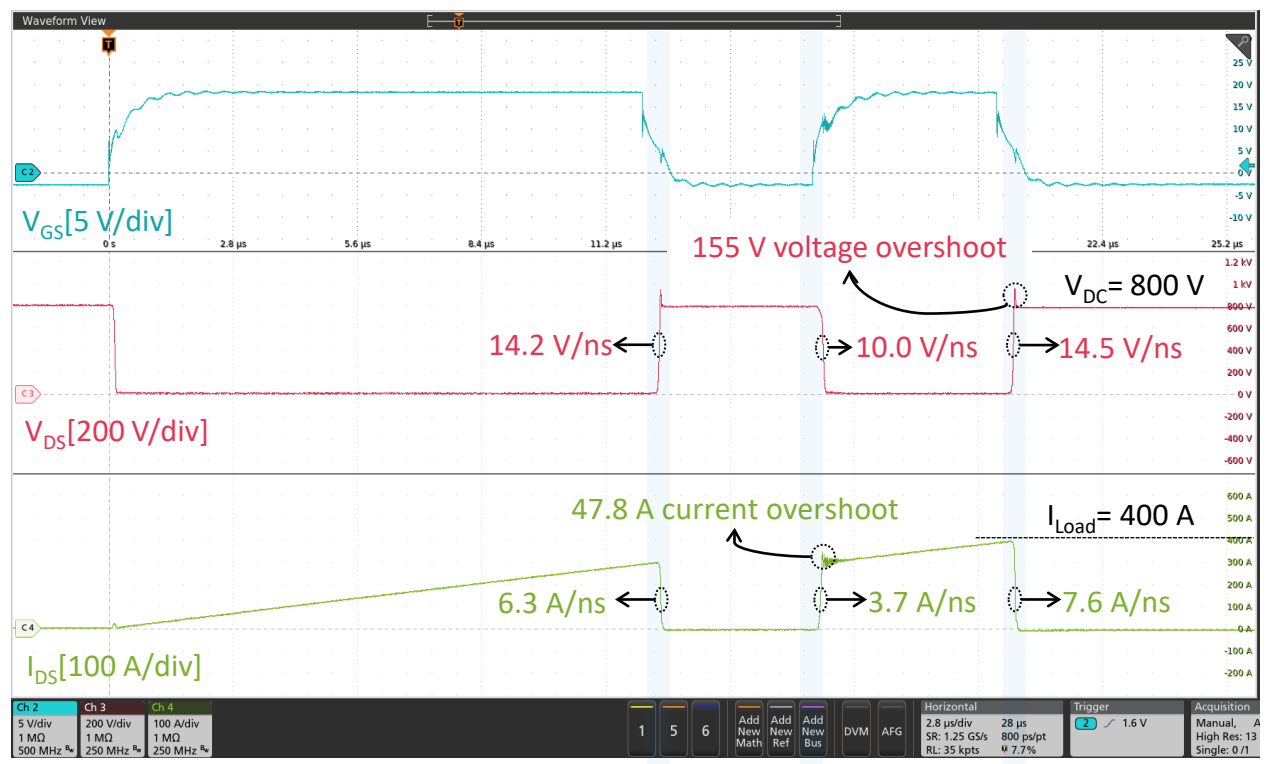


Typical Dynamic Performance of Modules (1)



Example Waveform of LS: 800 V, 400 A, 5 Ω, 25 °C

Example Waveform of HS: 800 V, 400 A, 5 Ω, 25 °C



$E_{off} @ 300 A = 9.5 \text{ mJ}$

$E_{on} @ 300 A = 14.4 \text{ mJ}$

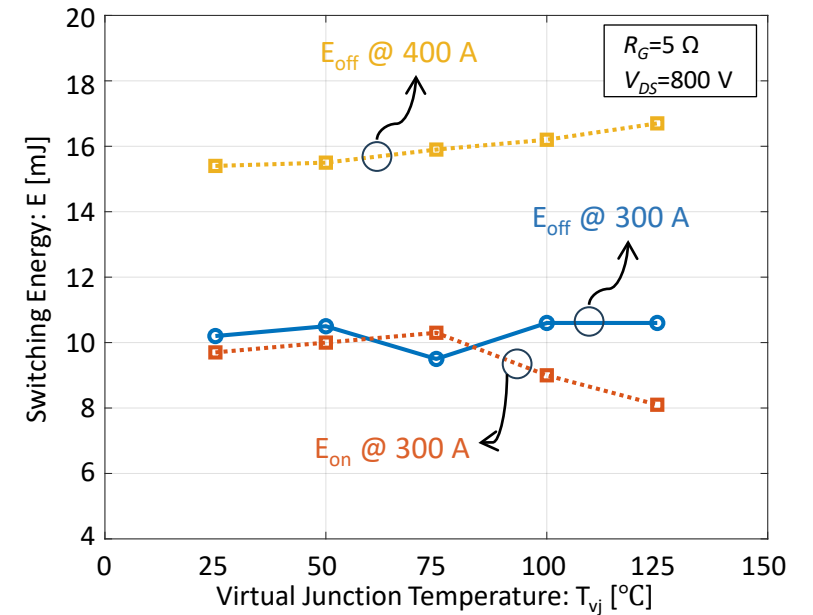
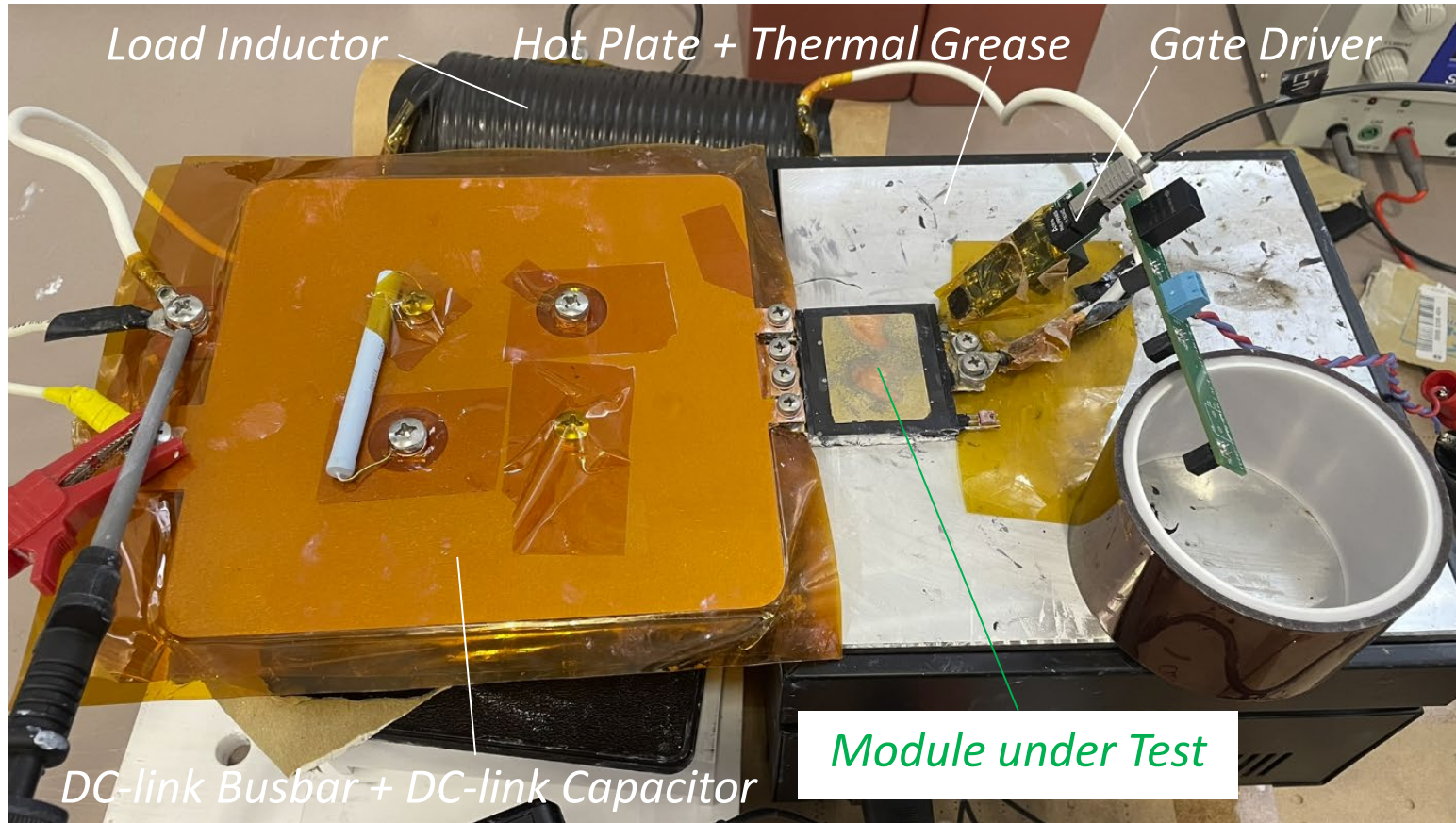
$E_{off} @ 400 A = 14.1 \text{ mJ}$

$E_{off} @ 300 A = 7.7 \text{ mJ}$

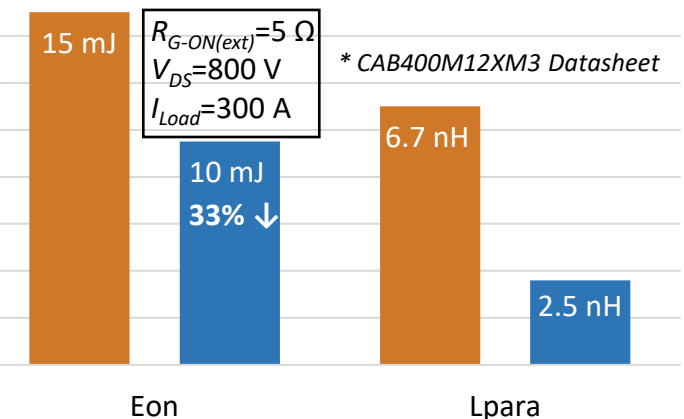
$E_{on} @ 300 A = 12.8 \text{ mJ}$

$E_{off} @ 400 A = 11.4 \text{ mJ}$

Typical Dynamic Performance of Modules (2)



- 1.2 kV/400 A SiC Module from Vendor A *
- Assembled 1.2 kV/400 A SiC Module



For the assembled modules :

- With $V_{GS} = -2 V / + 18 V$, $L_{load} = 30 \mu H$, $R_{G-ON(ext)} = R_{G-OFF(ext)} = 5 \Omega$, the turn-off energy E_{off} and turn-on energy E_{on} show a **slight temperature dependency over the entire temperature range**

Designed module packaging structure has the potential to utilize chip capabilities better

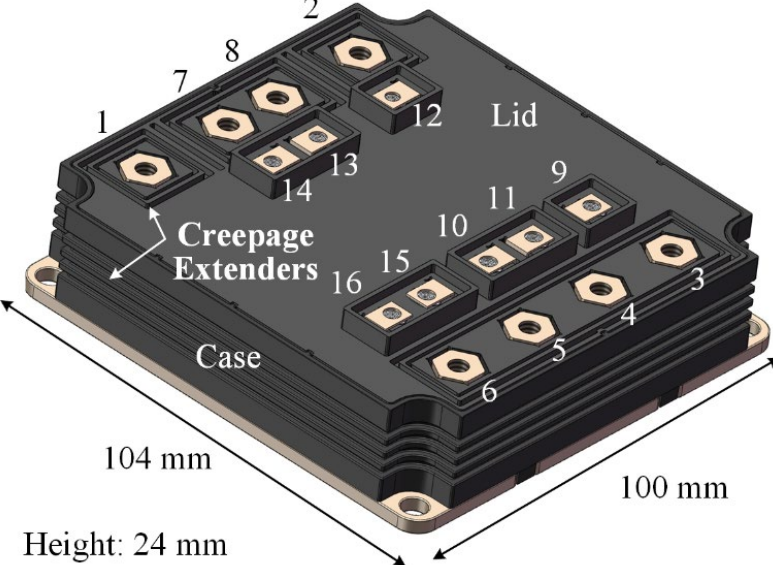
3.3 kV/200 A SiC Half-Bridge Power Module

-Pushing Boundaries of Single-Sided Structure with Functional Integration

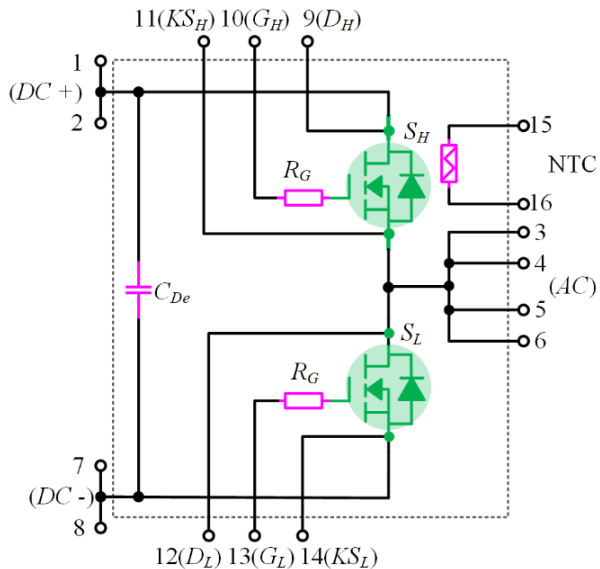
Functional Integration: Decoupling Caps.



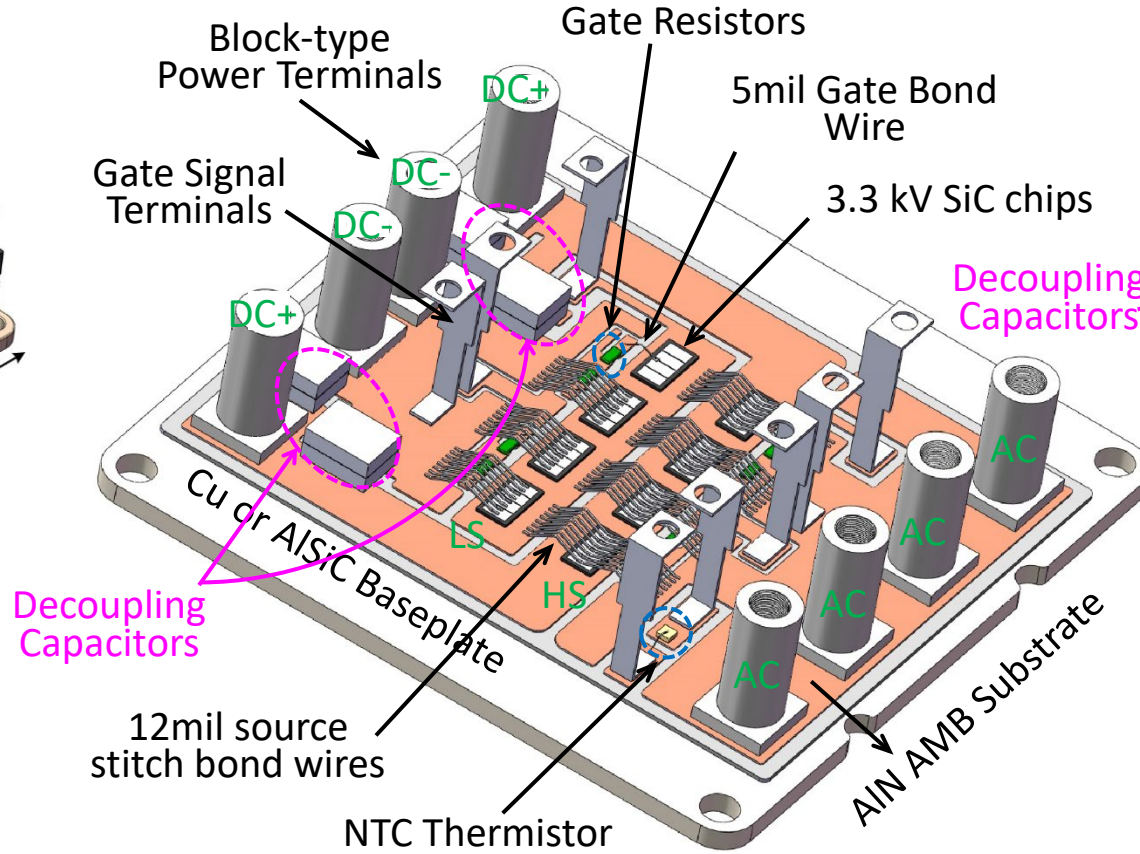
Module Appearance



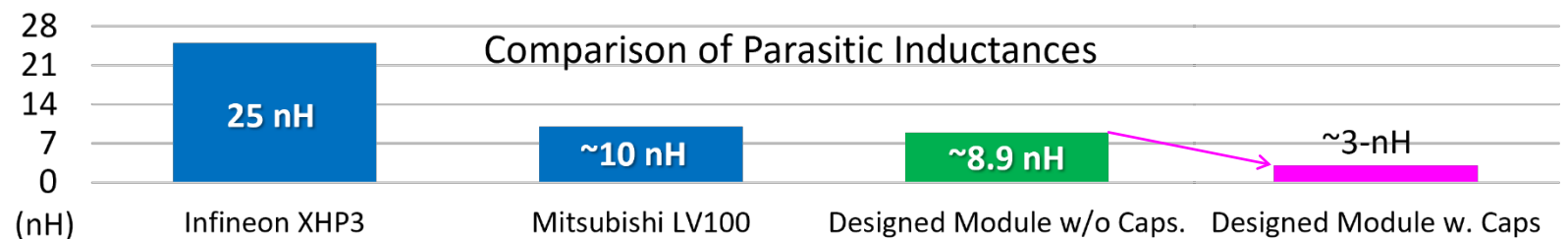
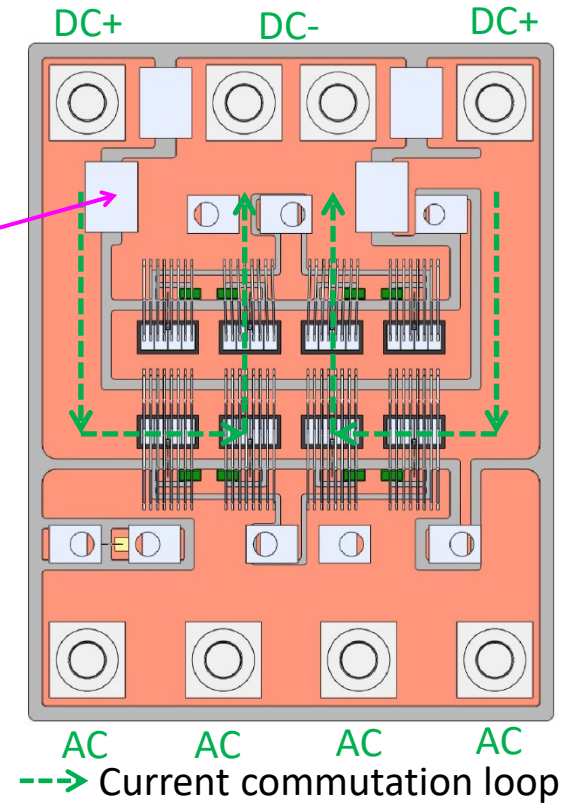
Module Schematic



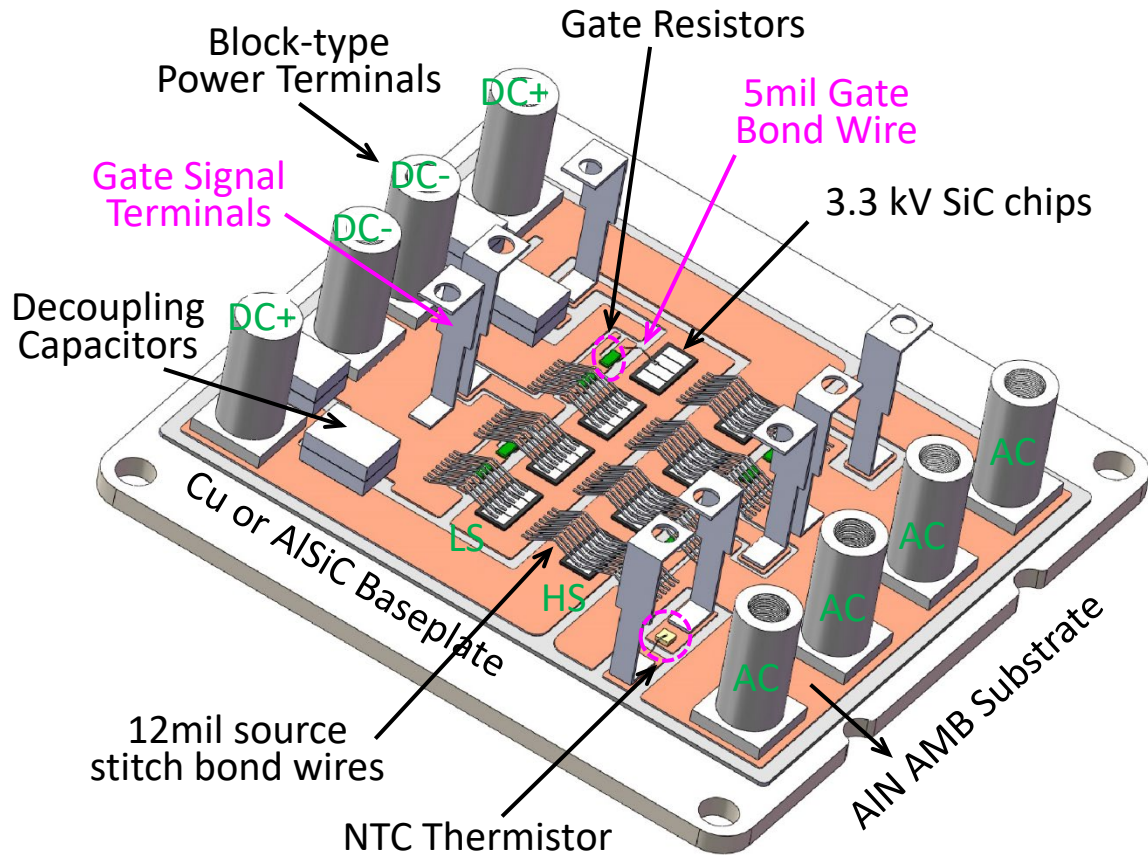
Internal Layout



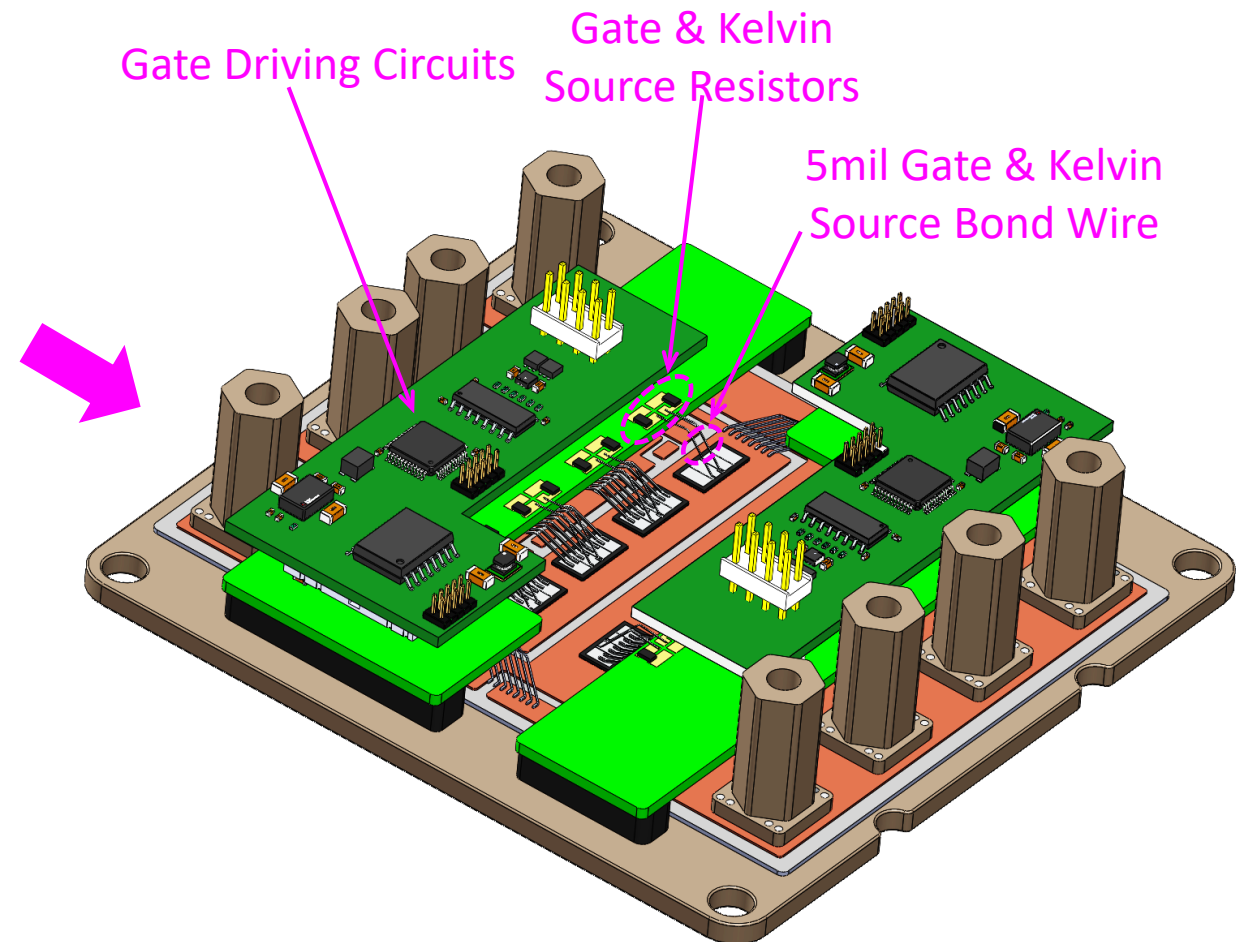
In-plane Substrate Layout



Functional Integration: Gate Drivers



Built-in gate drivers: Minimize gate-loop inductance and Maximize device performance



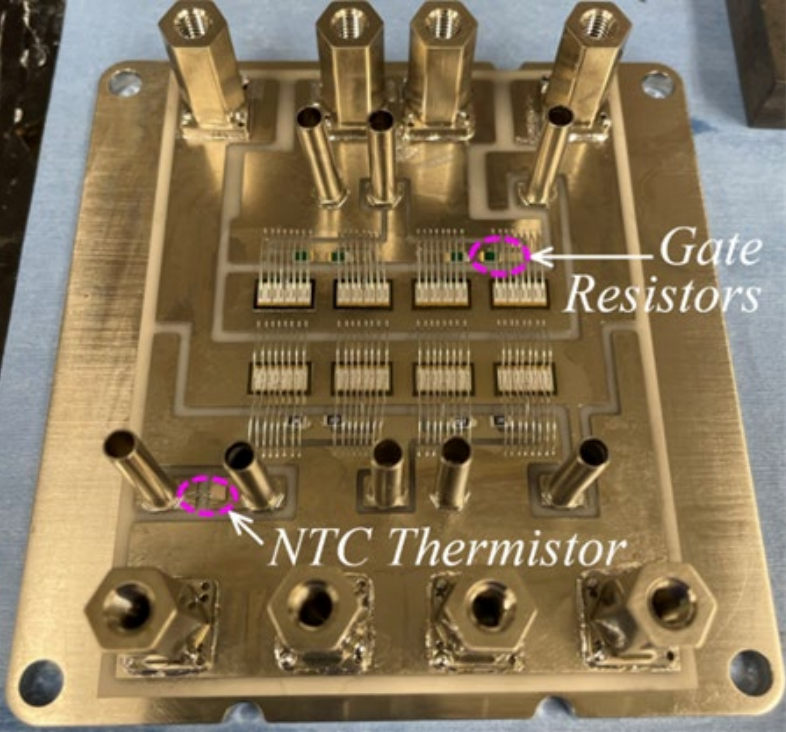
■ **Designed Module Stray Inductances (Q3D)**

Gate Loop	15 nH
Commutation Loop	8.9 nH w/o decoupling caps. 3 nH w. decoupling caps.

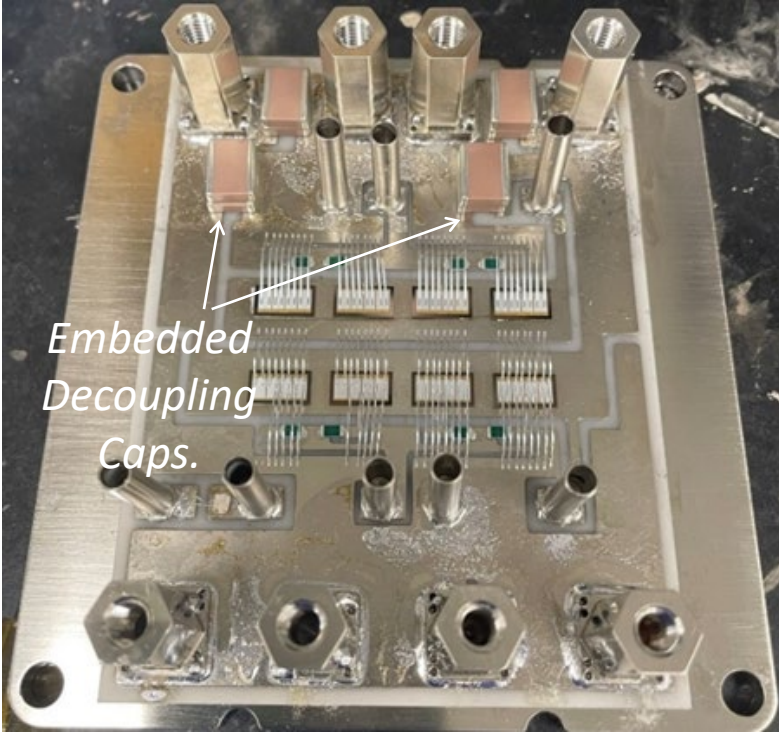
Assembled 3.3 kV/200 A Prototype Modules



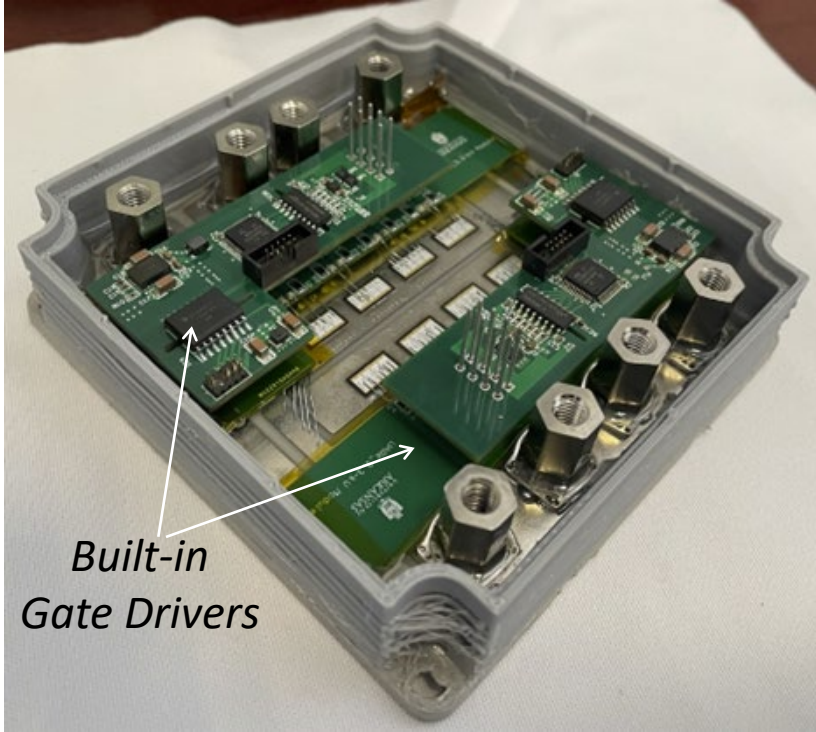
■ **Baseline Module**



■ **Module with Embedded Caps.**



■ **Module with Built-in Gate Driver**

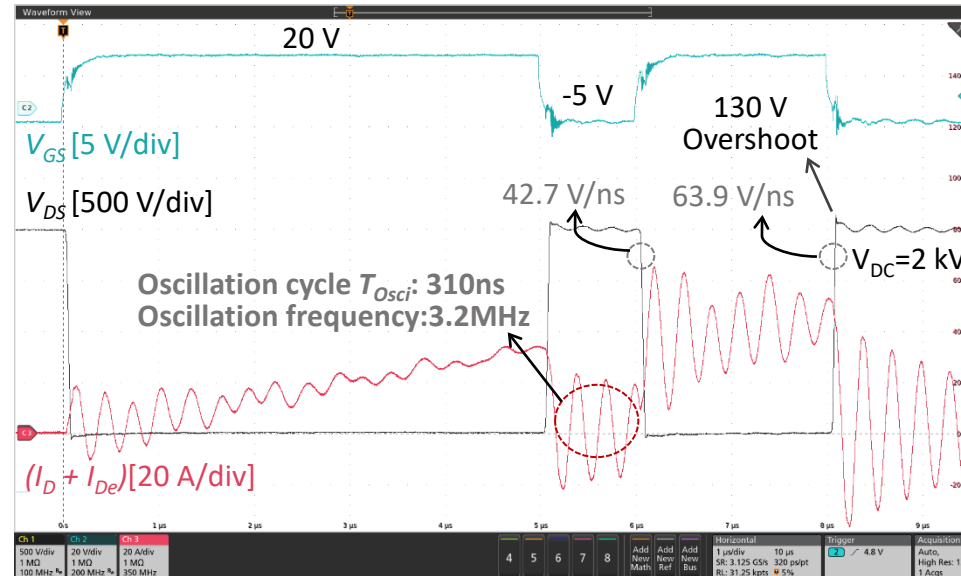
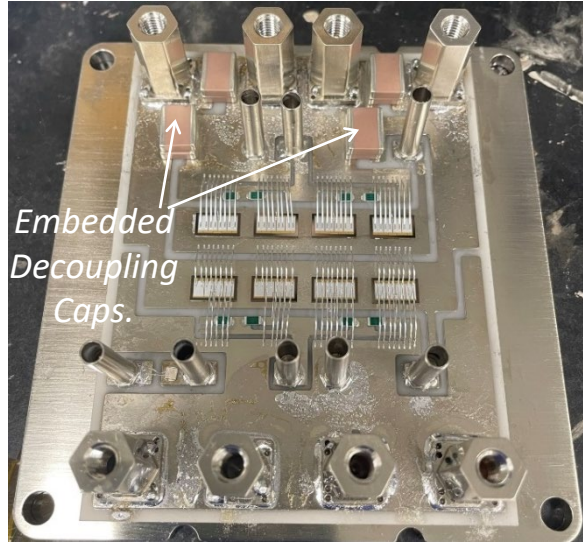


Performance Comparison and Demonstration

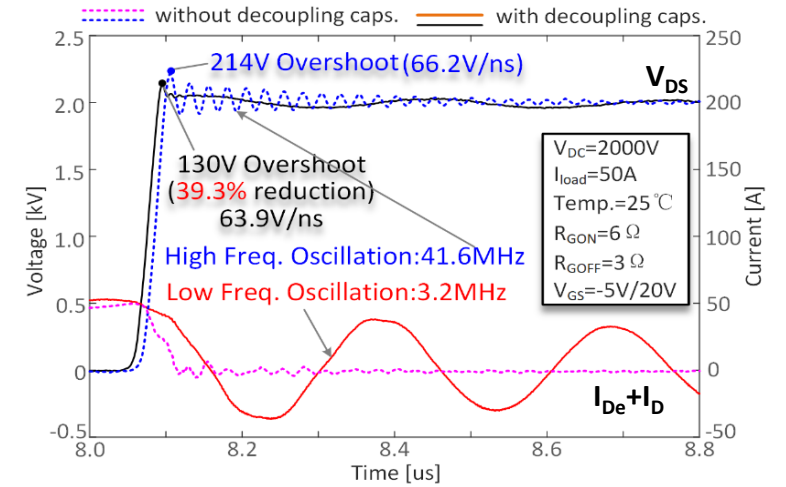


Module with Embedded Decoupling Capacitors

(Example Waveform: 2 kV, 50 A, 25 °C)



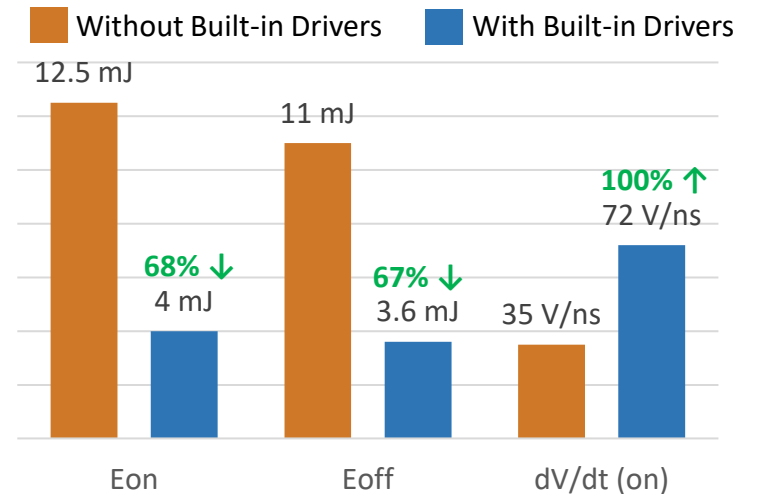
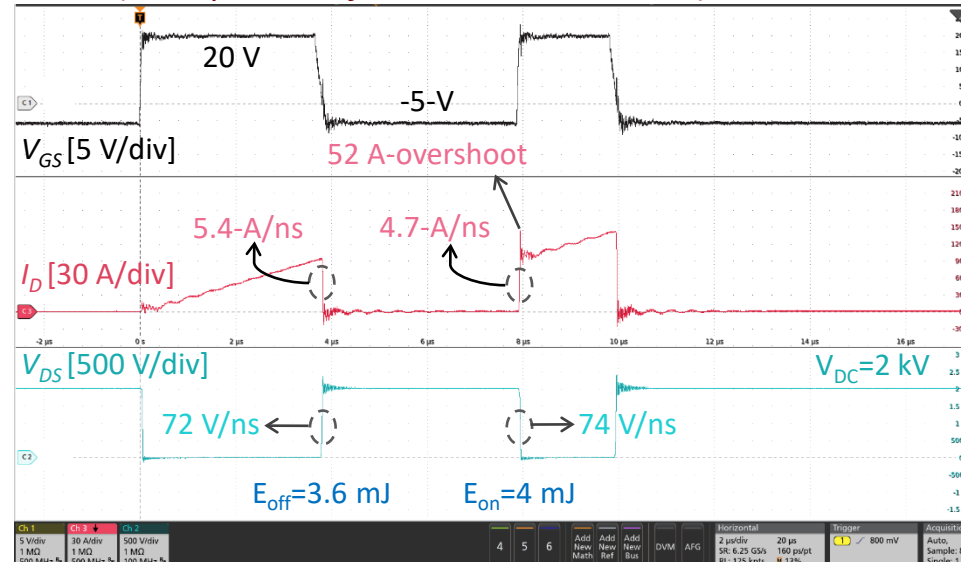
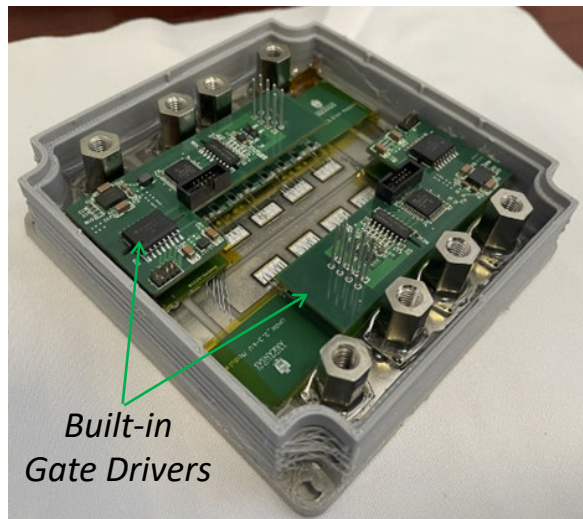
Comparison



Embedded decoupling Caps.: **Suppress** voltage overshoot, **difficult** to directly measure the current flow through chips

Module with Built-in Gate Drivers

(Example Waveform: 2 kV, 150 A, 25 °C)



Built-in gate driver: can **maximize** device performance 14

- More research should be extended from WBG device technology to **WBG power module packaging development**, encompassing all necessary technologies and supply steps along the value chain of WBG power electronics.
- To **maximize** SiC device performance,
 - **Advanced structures**: wire bondless, double-sided cooled...
 - **Functional integration** to push the boundaries of traditional single sided structures

Thank you !