Advancements in High Voltage SiC Power Devices: From 3.3kV to Beyond 10kV

Power Electronics and Energy Conversion Workshop

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Army Research Lab (Dr. Aivars Lelis and Dr. Miguel Hinojosa)
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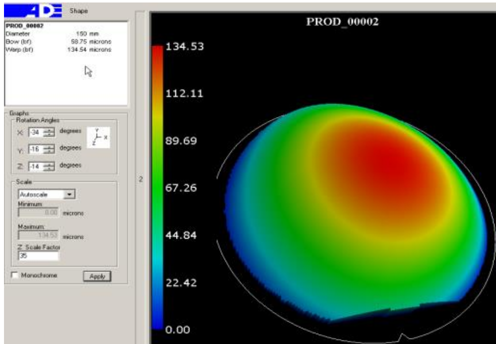
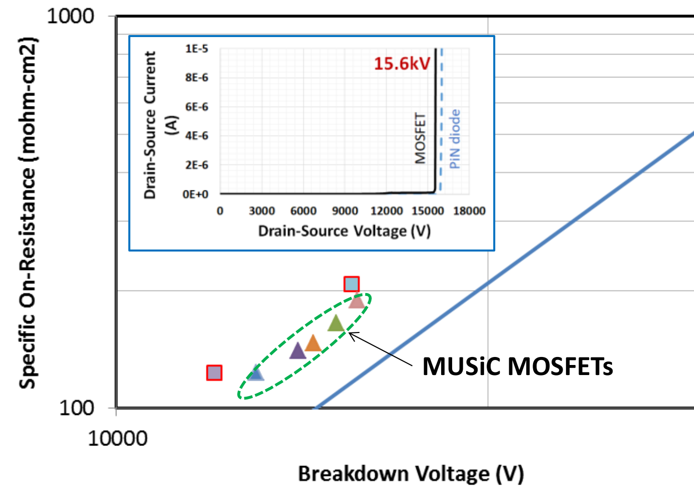
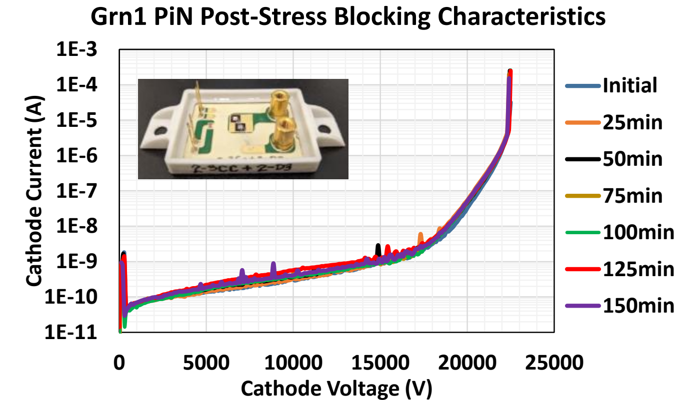
Recent research on >10kV Devices







2018, 2019

10kV rated SiC MOSFETs, JBSFETs, Ni-JBS, Ti-JBS

Fabricated at X-FAB

Wafers were scrapped due to severe physical deformation

2019 – 2021

15kV SiC MOSFETs, JBSFETs

Fabricated at Analog Devices (Hillview, CA)

Demonstrated record trade-off between Ron and BV

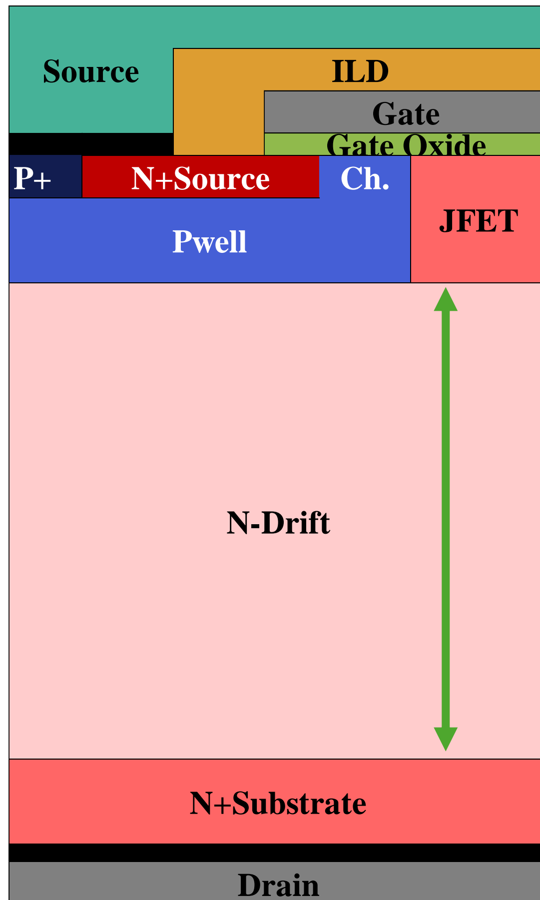
2023

23kV SiC PiN diodes

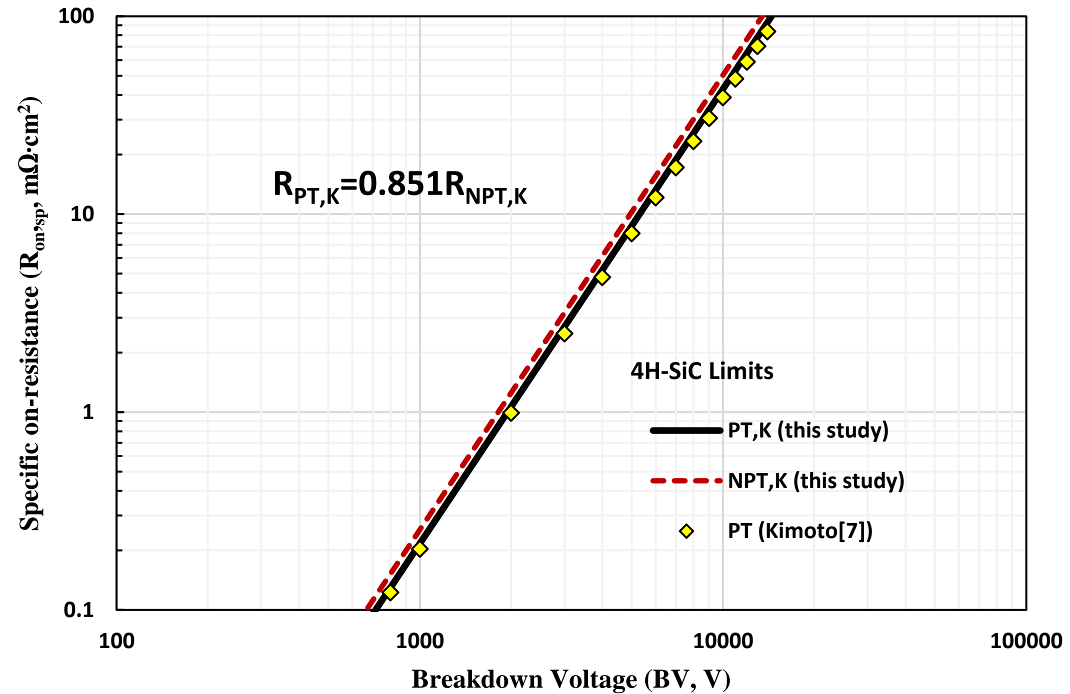
Fabricated at SiCamore (Bend, Oregon)

Demonstrated PiN diodes with near-ideal breakdown voltages

Drift layer design



High Voltage MOSFET Schematic



S. B. Isukapati and W. Sung, "An Efficient Design Approach to Optimize the Drift Layer of Unipolar Power Devices in 4H-SiC," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 176-181, 2020, doi: 10.1109/JEDS.2020.2973675
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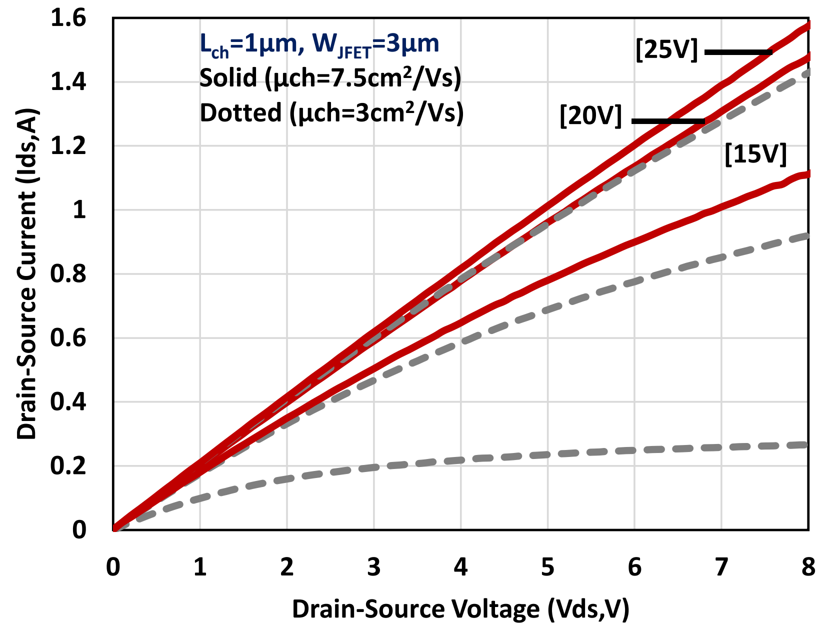
~ **15% reduction** of Drift Resistance with proper drift design.

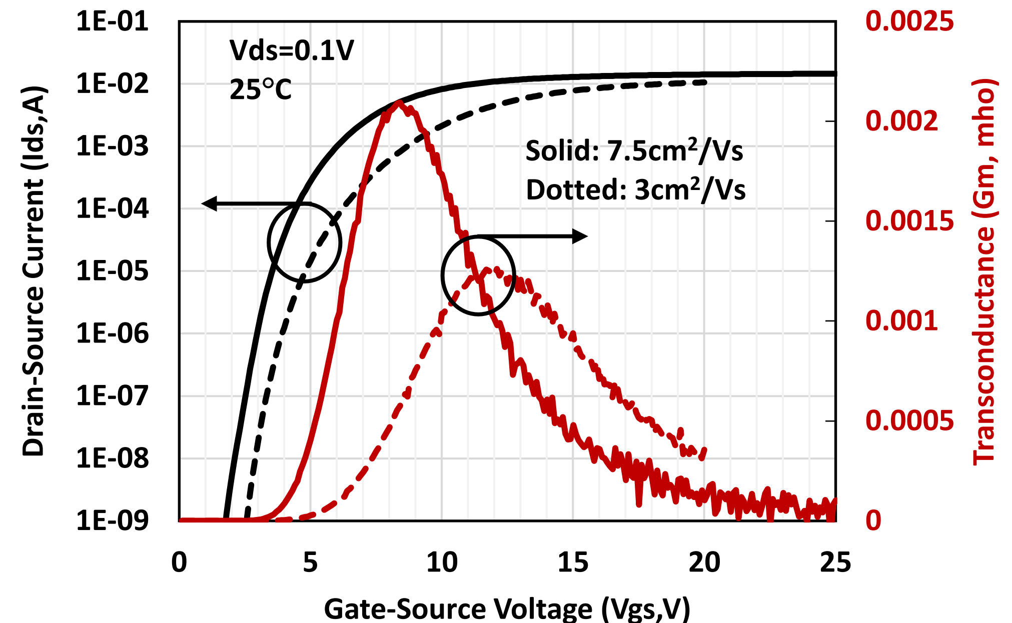
Resistance in HV device structure

N. Yun et al., "Developing 13-kV 4H-SiC MOSFETs: Significance of Implant Straggle, Channel Design, and MOS Process on Static Performance," in IEEE Transactions on Electron Devices, vol. 67, no. 10, pp. 4346-4353, Oct. 2020, doi: 10.1109/TED.2020.3017150.

Drift resistance breakdown at various voltage ratings.

Voltage Rating	Drift Layer Width (μm)	Drift Layer Doping (cm^{-3})	Drift Resistance ($m\Omega{*}cm^2$)	Device Resistance ($m\Omega{*}cm^2$)	Drift Resistance %
1.2 kV	10	8.00E+15	0.78	3.13	24.91
6.5 kV	60	1.00E+15	34.15	37.59	90.86
15 kV	145	5.00E+14	162.94	170.91	95.34

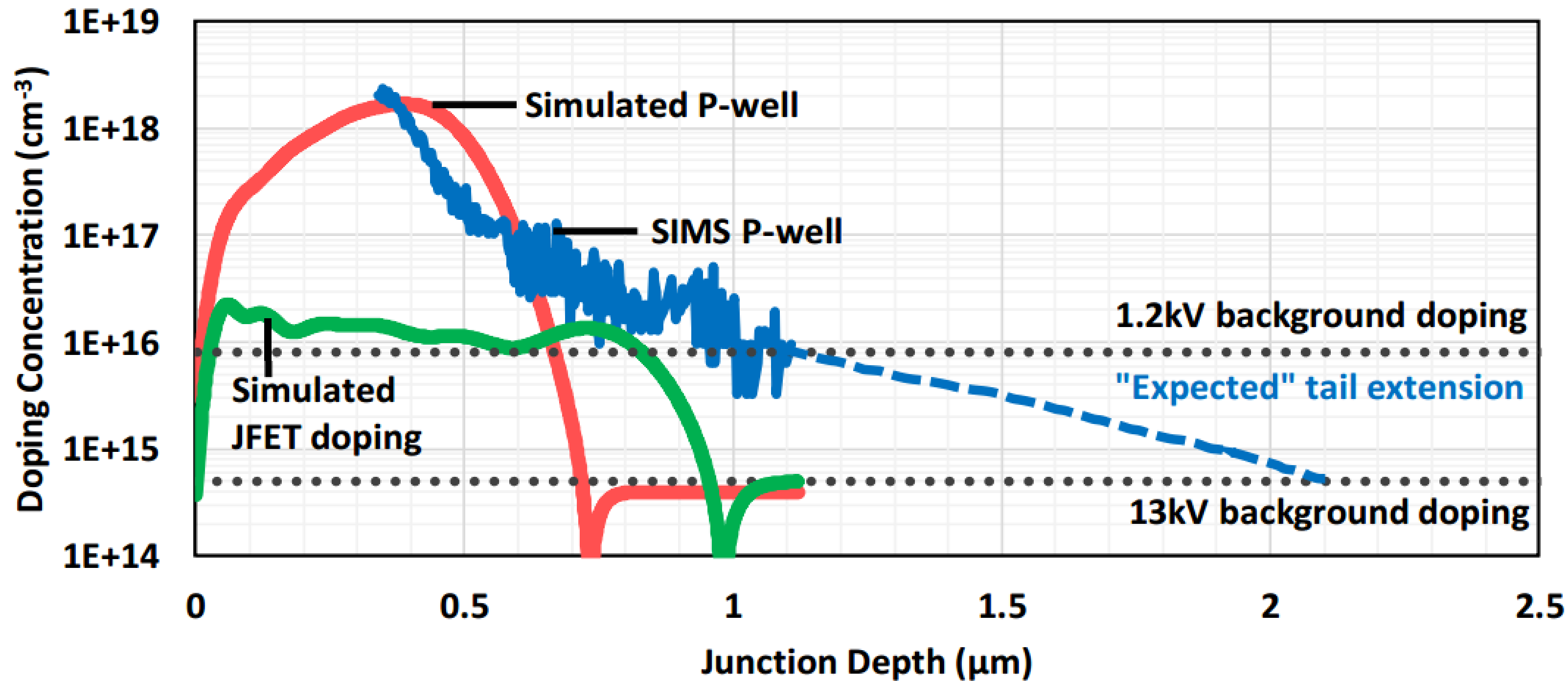


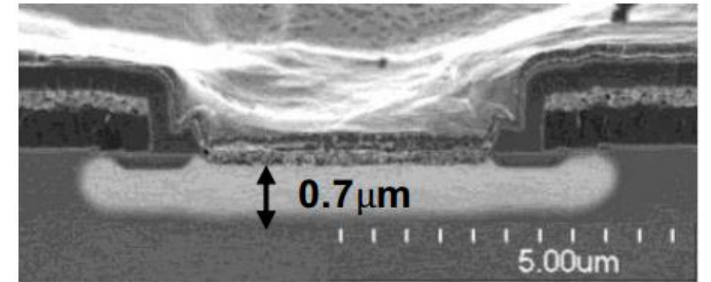


Specific Ron = 200 $m\Omega$-cm^2 [V_{gs}=20V]
(compare with 241 $m\Omega$-cm^2 with low μ_{ch})

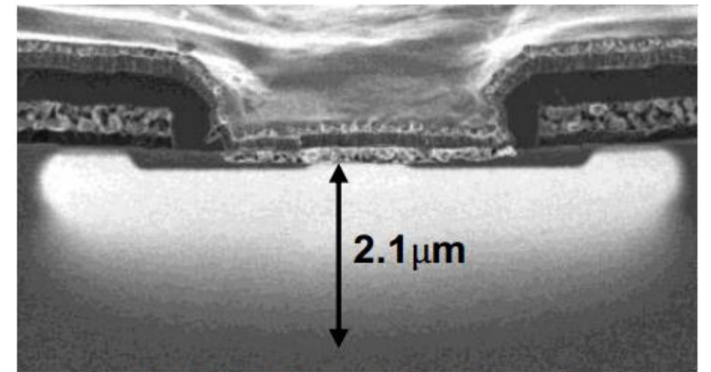
Threshold voltage = 4V
@ Ids = 100μA [V_{ds}=0.1V]
(Compare with 6V with low μ_{ch})

Junction formation in HV devices





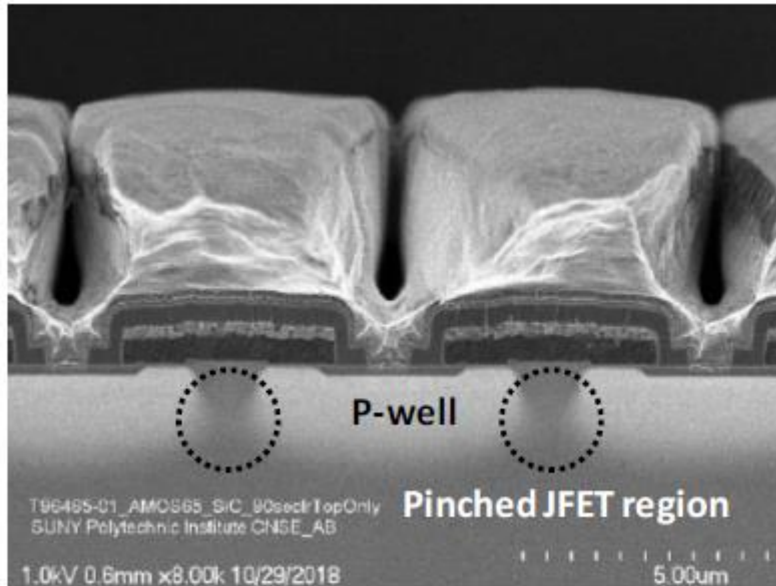
1.2kV MOSFET's P-well



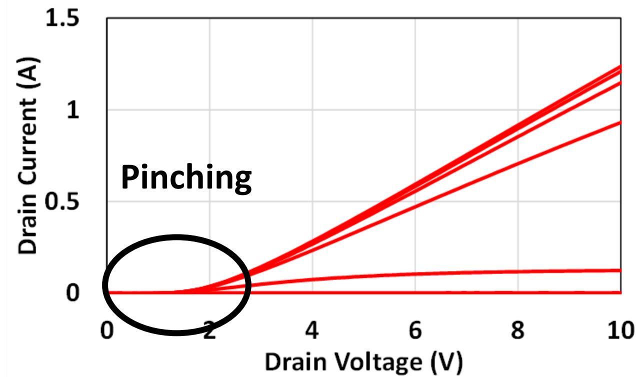
13kV MOSFET's P-well

- Different from LV devices, Implant straggle is excessive in lightly doped epi-layer for HV devices
- Impact on both forward conduction as well as blocking behaviors;

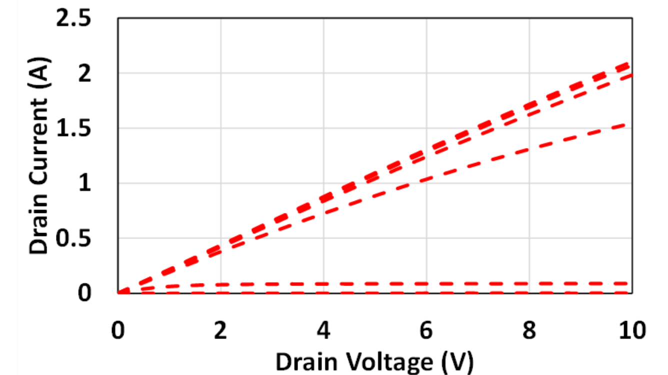
Output characteristics and solutions



HV MOSFET SEM Image showing large increase in implantation straggle.



MOSFET output with pinched JFET.



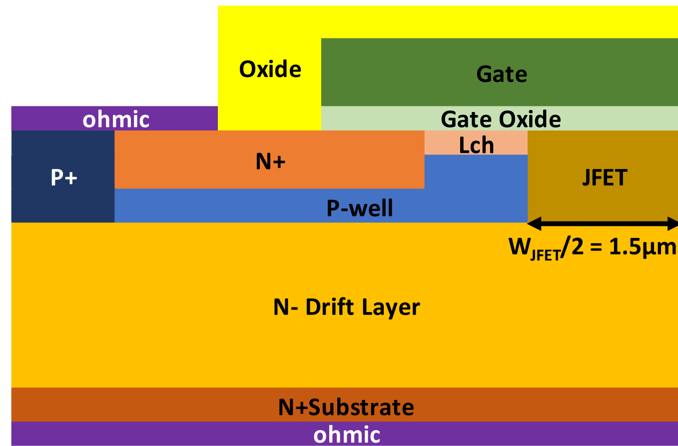
MOSFET output with proper JFET width.

N. Yun et al., "Developing 13-kV 4H-SiC MOSFETs: Significance of Implant Straggle, Channel Design, and MOS Process on Static Performance," in IEEE Transactions on Electron Devices, vol. 67, no. 10, pp. 4346-4353, Oct. 2020, doi: 10.1109/TED.2020.3017150.

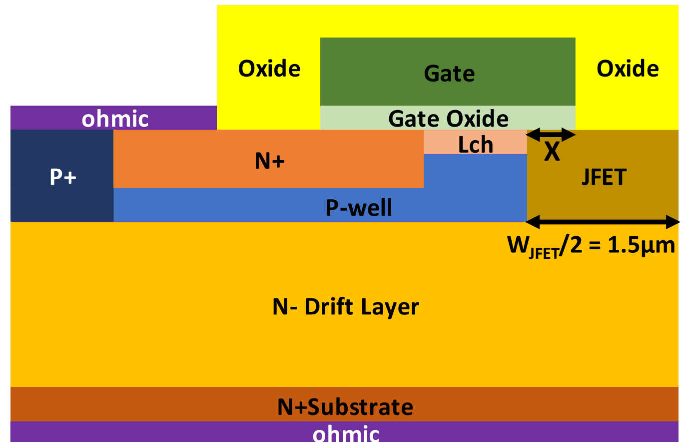
J. Lynch, et al., "Design Considerations for High Voltage SiC Power Devices: An Experimental Investigation into Channel Pinching of 10kV SiC Junction Barrier Schottky (JBS) Diodes," 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 2019, pp. 223-226, doi: 10.1109/ISPSD.2019.8757593.

- Proper JFET width is required to prevent JFET channel pinching.
- Enhanced doping in the JFET region and Pwell formation within the JFET region is required.

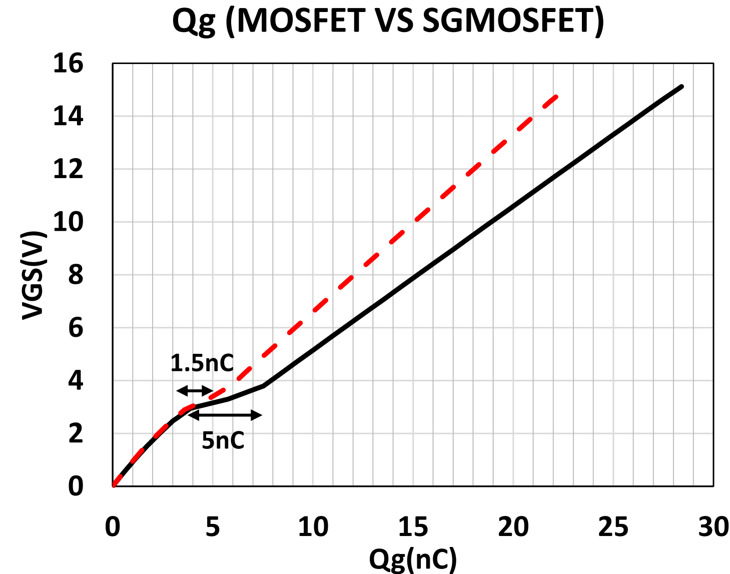
15kV Split Gate MOSFET



Schematic Diagram of a traditional HV MOSFET



Schematic Diagram of a HV SG-MOSFET

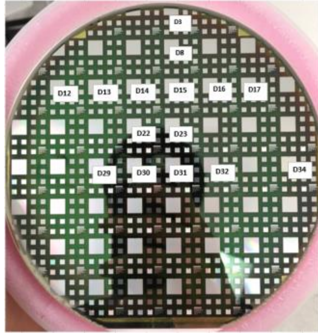


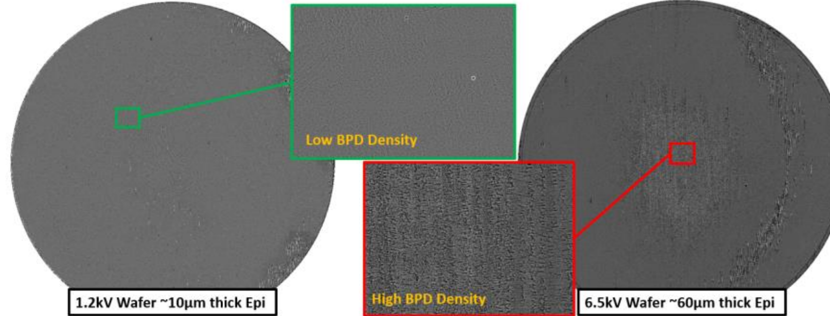
Measured gate charge of the conventional MOSFET (black) and SG-MOSFET (red)

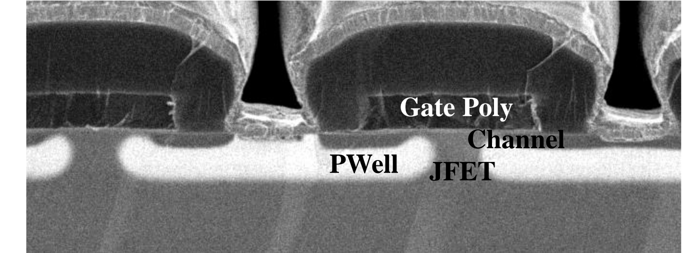
Structure	MOSFET	SG-MOSFET
Ron,sp @ BV=12kV	204 mΩcm²	200 mΩcm²
Ron,sp @ BV=15kV	273 mΩcm²	281 mΩcm²
Lowest Ron,sp	183 mΩcm²	189 mΩcm²
BV of Lowest Ron,sp	11600 V	11600 V
Gate Charge	5 nC	1.5 nC

Justin Lynch, Nick Yun, Woongje Sung, Igal Deckman, Dennis Rossman, Sung Kim, Duy-son Nguyen, Jin-Ho Seo, Daniel Haberstat, Miguel Hinojosa, Ronald Green, and Aivars Lelis, “Demonstration of High Voltage (15kV) Split-Gate 4H-SiC MOSFETs,” Proceedings of Wide Bandgap Power Devices & Applications (WiPDA), November 2021, doi: 10.1109/WiPDA49284.2021.9645153

Recent research on 6.5kV Devices







2018, 2019

6.5kV rated SiC MOSFETs, JBSFETs, Ni-JBS, Ti-JBS
Fabricated at X-FAB

1st lot (2018): design errors, low BV
2nd lot (2019): demonstrated all devices

2021

6.5kV rated SiC MOSFETs, JBSFETs, Ti-JBS
Fabricated at Analog Devices (Hillview, CA)
Process issue (Gate-Source short)
Material issue: Extremely low yield

2023

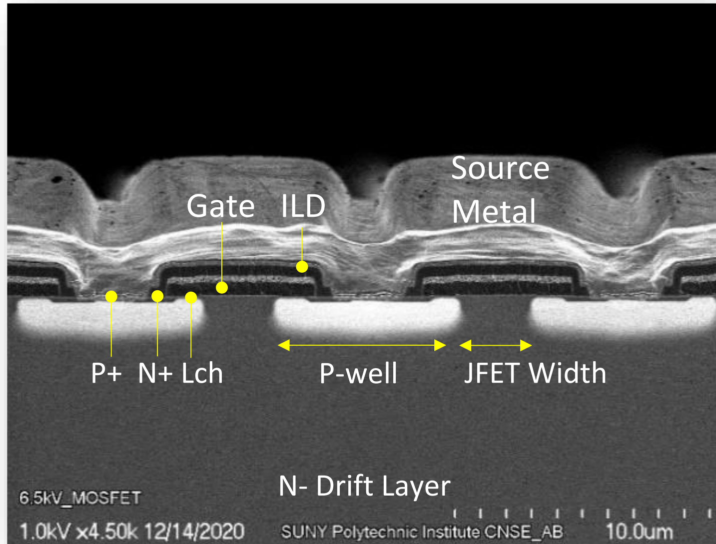
6.5kV rated SiC MOSFETs, JBSFETs, Ti-JBS
Fabricated at SiCamore (Bend, Oregon)

Demonstrated deep P-well with channeling, One-channel MOSFET

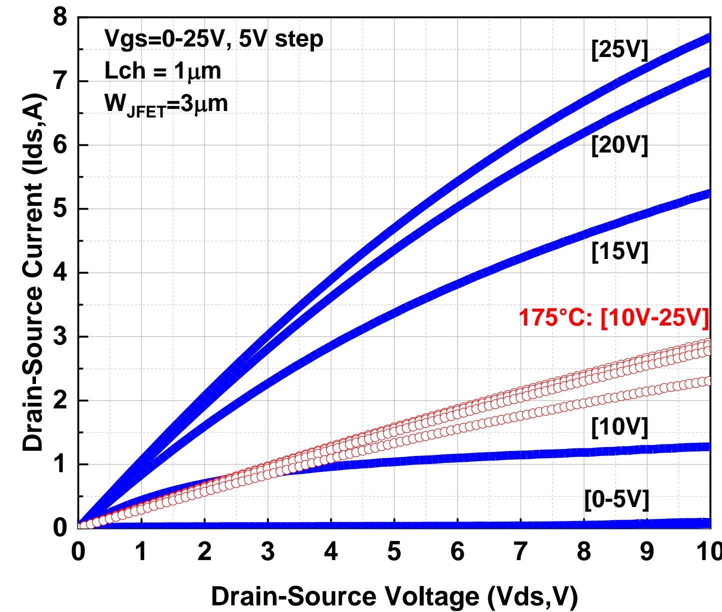
R. Stahlbush *et al*., "Defects in 4H-SiC epilayers affecting device yield and reliability," *2022 IEEE International Reliability Physics Symposium (IRPS)*, 2022, pp. P65-1-P65-6, doi: 10.1109/IRPS48227.2022.9764473.

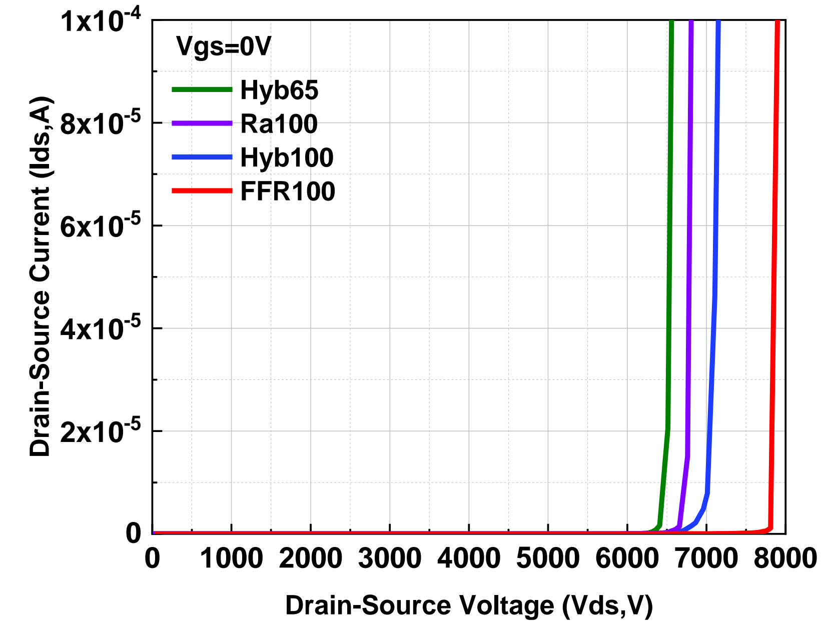
6.5kV SiC MOSFETs

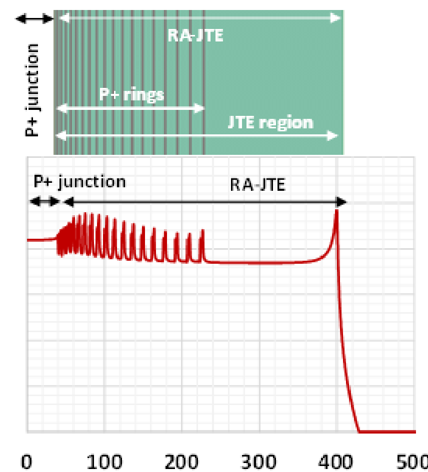
N. Yun, J. Lynch, S. DeBoer,A. J. Morgan, D. Xing, M. Kang, A, Agarwal, V. Veliadis, V. Amarasinghe, and J. Ransom, "Critical Design Considerations for Static and Dynamic Performances on 6.5 kV 4H-SiC MOSFETs Fabricated in a 6-inch SiC Foundry," in 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Nov. 2021, pp. 361–365. doi: 10.1109/WiPDA49284.2021.9645146.

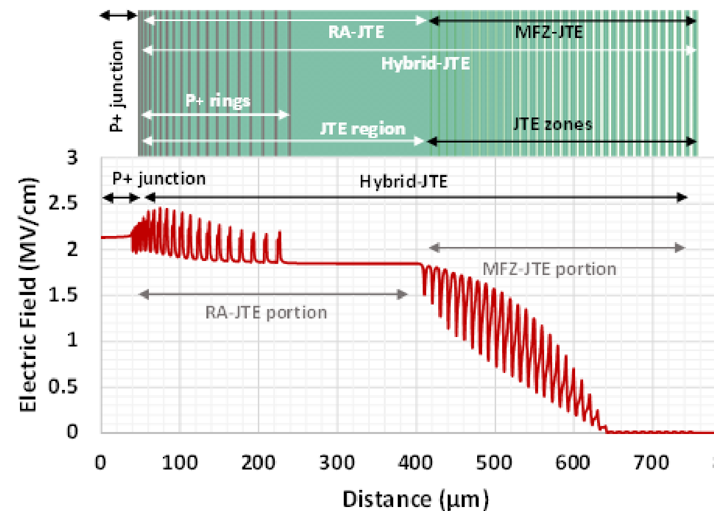


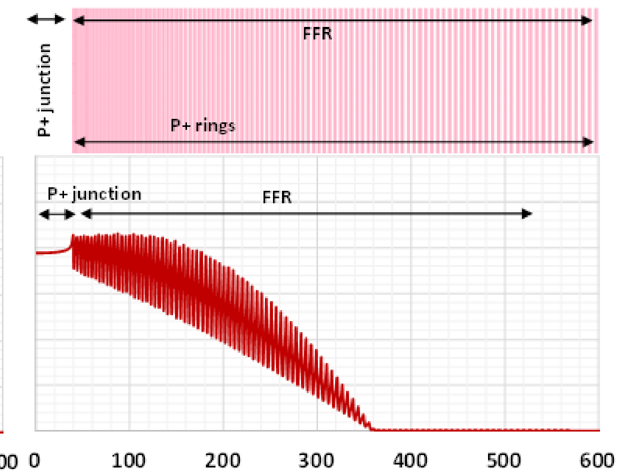
Fabricated at X-FAB, 2019





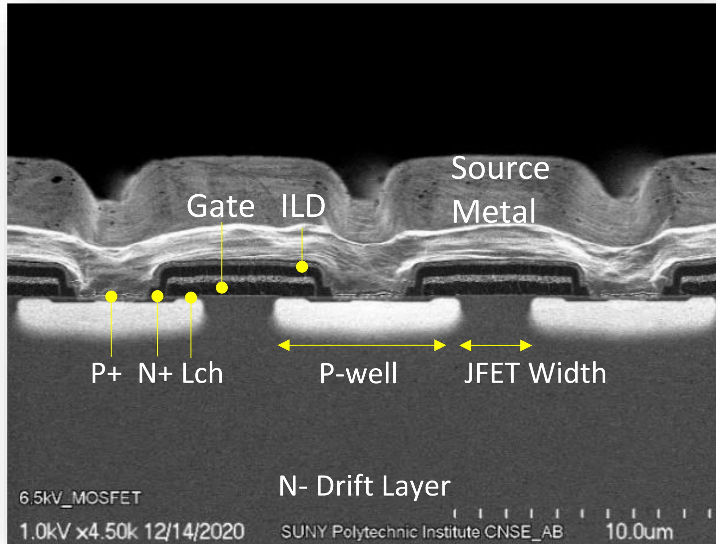




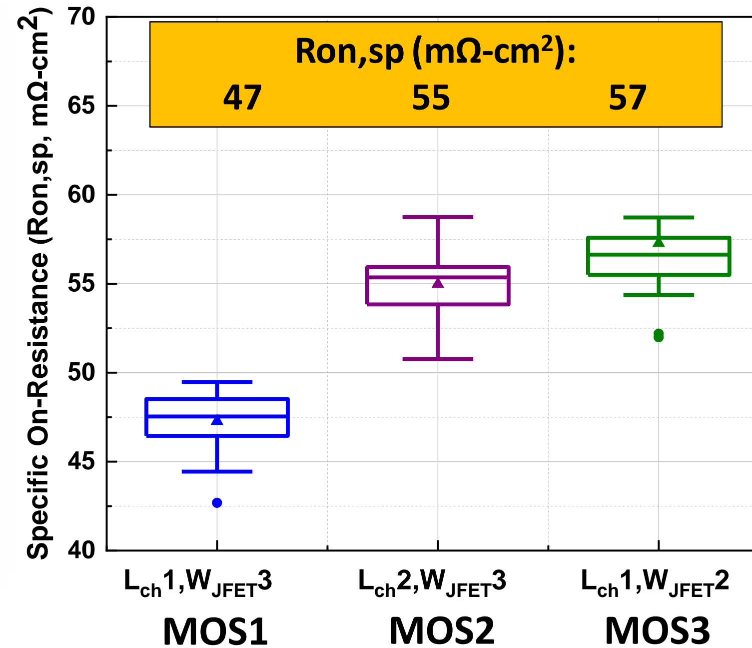


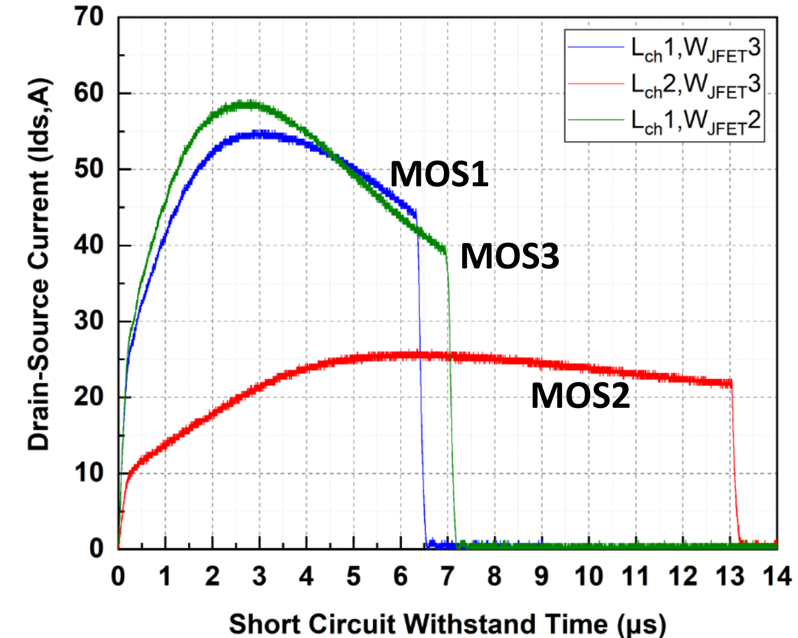
6.5kV SiC MOSFETs

N. Yun, J. Lynch, S. DeBoer,A. J. Morgan, D. Xing, M. Kang, A, Agarwal, V. Veliadis, V. Amarasinghe, and J. Ransom, “Critical Design Considerations for Static and Dynamic Performances on 6.5 kV 4H-SiC MOSFETs Fabricated in a 6-inch SiC Foundry,” in 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Nov. 2021, pp. 361–365. doi: 10.1109/WiPDA49284.2021.9645146.



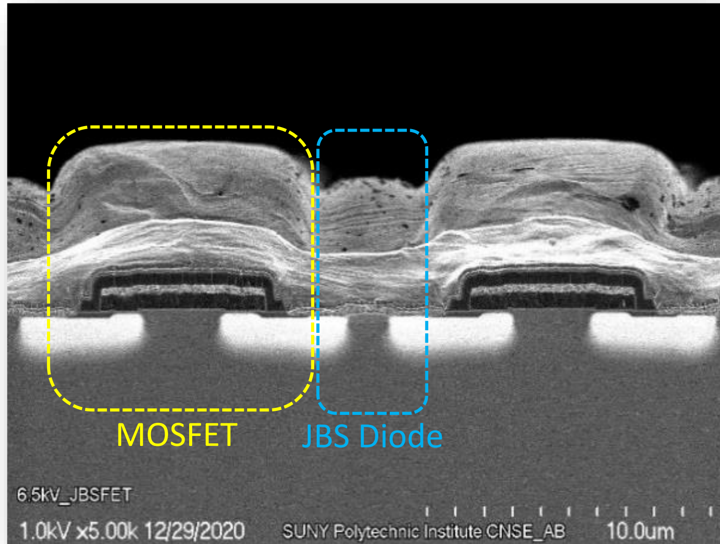
Fabricated at X-FAB, 2019



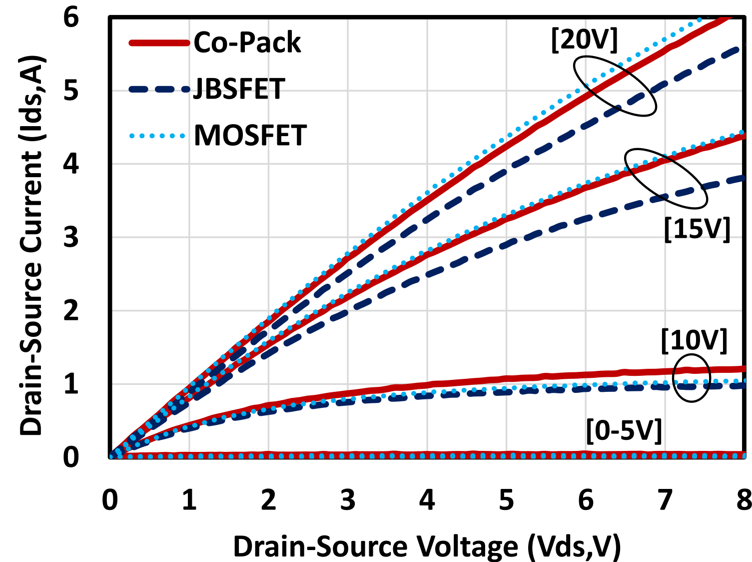


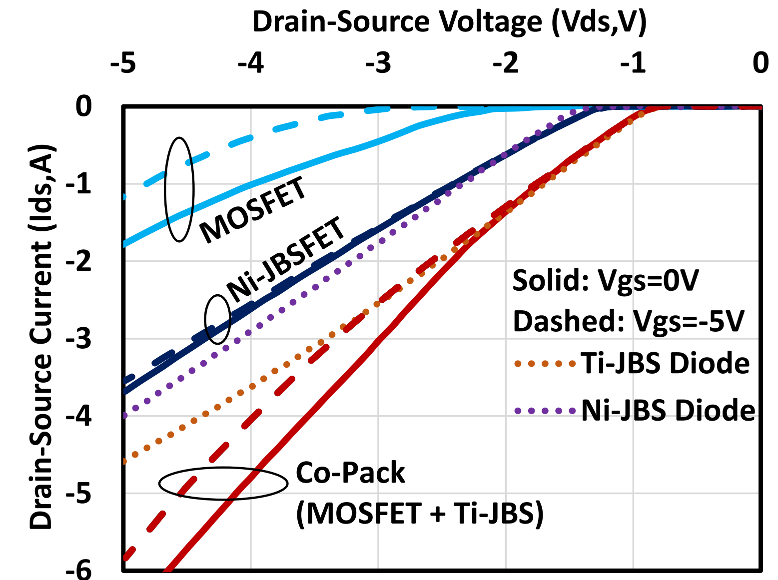
- Channel length and JFET width majorly determine the on-resistance.
- Smaller cell-pitch can further reduce the on-resistance.
- Longer channel length and narrower JFET width improve the short circuit withstand capability. Comparing MOS1 and MOS2, SCWT is 2x improved, but there is only 15% increase in Ron,sp.

6.5kV JBSFET (JBS diode integrated MOSFET)



JBSFET: JBS diode integrated MOSFET

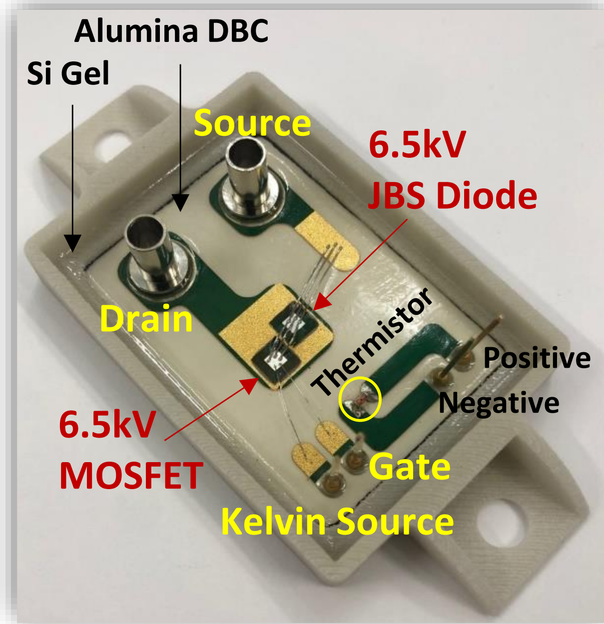


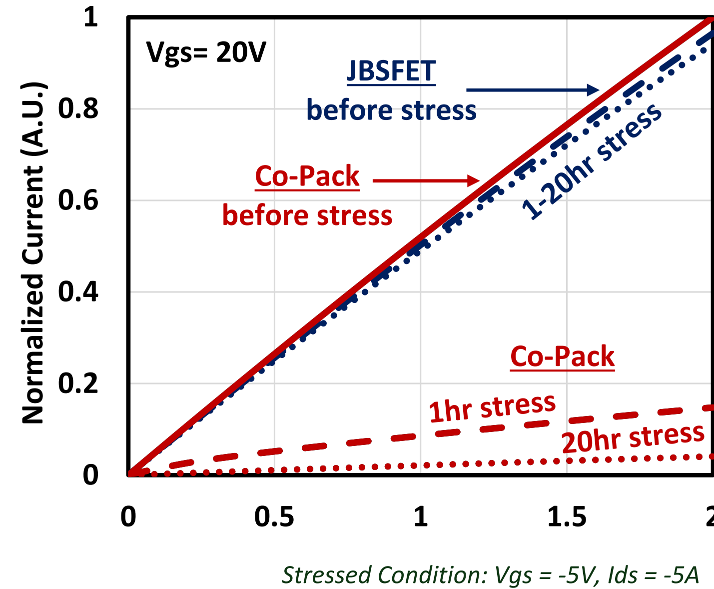


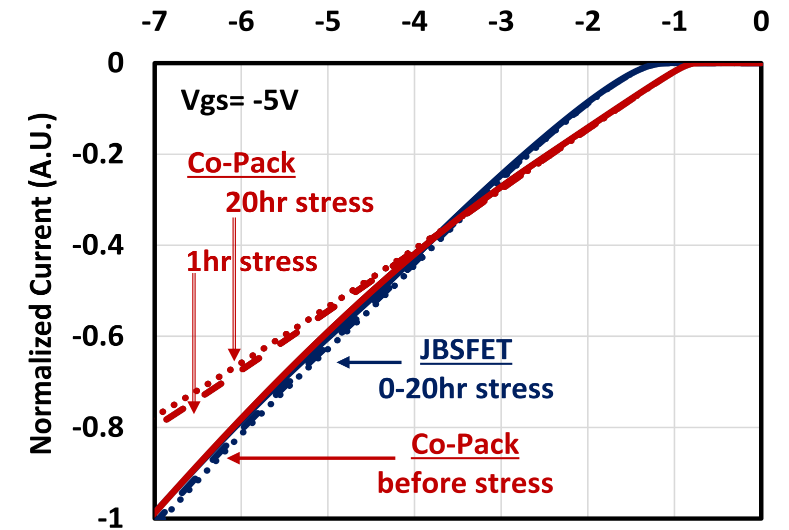
- JBSFET was proposed to disable the operation of body diode – no BPD induced degradation.
- Schottky region is allocated within MOSFET cell, interrupting Pwell.
- In 3rd quadrant operation, JBSFET exhibit lower Vth than MOSFET and enjoy unipolar current conduction.
- No freewheeling diode is required saving significant wafer area.

N. Yun, J. Lynch, A. J. Morgan, D. Xing, M. Jin, J. Qian, M. Kang, V. Amarasinghe, J. Ransom, and V. Veliadis., "Comparative Study of 6.5 kV 4H-SiC Discrete Packaged MOSFET, JBSFET, and Co-Pack (MOSFET and JBS Diode)," in 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 2022, pp. 249–252. doi: 10.1109/ISPSD49238.2022.9813639.

6.5kV MOSFET vs JBSFET – Ruggedness





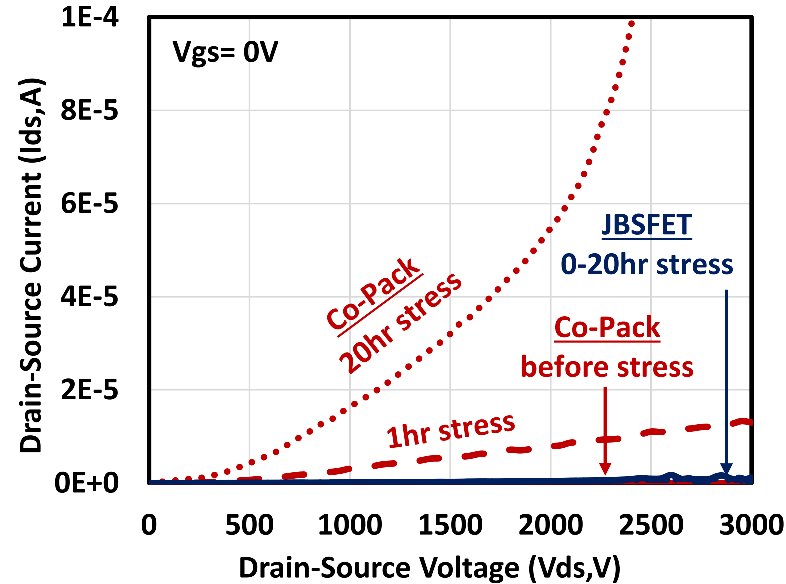


Stressed Condition: Vgs = -5V, Ids = -5A

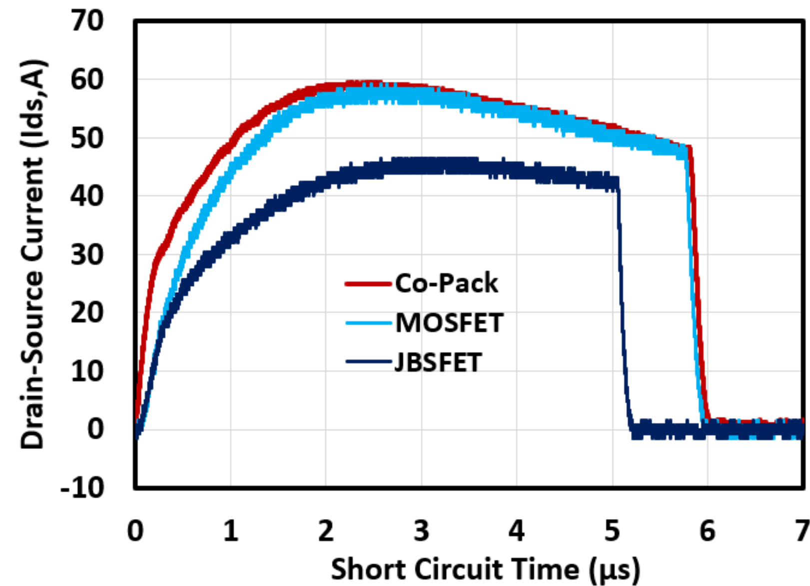
- JBSFET and Co-pack (MOSFET + JBS diode) were compared before/after diode stress test.
- Co-pack shows significant degradation in output characteristics and 3Q diode behavior.
- This is believed to be originated from body diode conduction in Co-Pack or MOSFET.

N. Yun, J. Lynch, A. J. Morgan, D. Xing, M. Jin, J. Qian, M. Kang, V. Amarasinghe, J. Ransom, and V. Veliadis., “Comparative Study of 6.5 kV 4H-SiC Discrete Packaged MOSFET, JBSFET, and Co-Pack (MOSFET and JBS Diode),” in 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 2022, pp. 249–252. doi: 10.1109/ISPSD49238.2022.9813639.

6.5kV MOSFET vs JBSFET – Ruggedness



Stressed Condition: Vgs = -5V, Ids = -5A

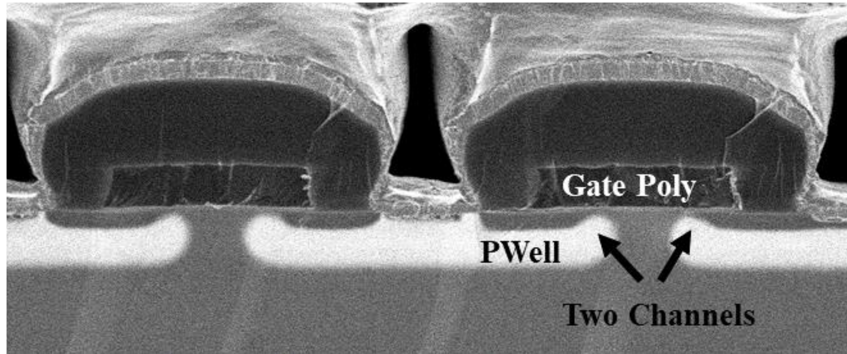


Test Condition: Vgs = 20V, Vds = 3.5kV

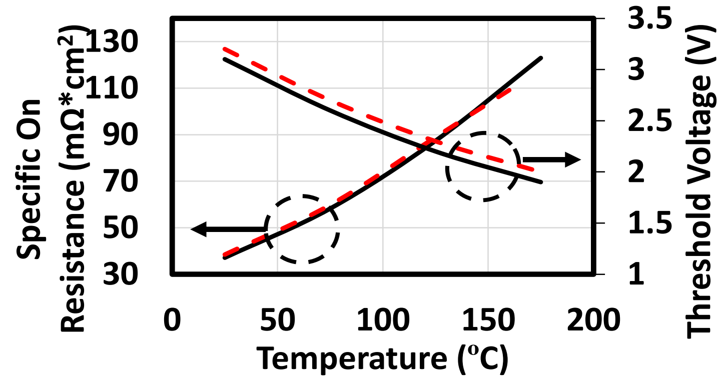
- Significant increase in leakage current is observed from Co-pack while JBSFET showed negligible shift.
- One drawback using JBSFET is shorter short circuit time (6 us vs 5 us).
- Originated from large leakage due to Schottky barrier lowing at high temperature.

N. Yun, J. Lynch, A. J. Morgan, D. Xing, M. Jin, J. Qian, M. Kang, V. Amarasinghe, J. Ransom, and V. Veliadis., “Comparative Study of 6.5 kV 4H-SiC Discrete Packaged MOSFET, JBSFET, and Co-Pack (MOSFET and JBS Diode),” in 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 2022, pp. 249–252. doi: 10.1109/ISPSD49238.2022.9813639.

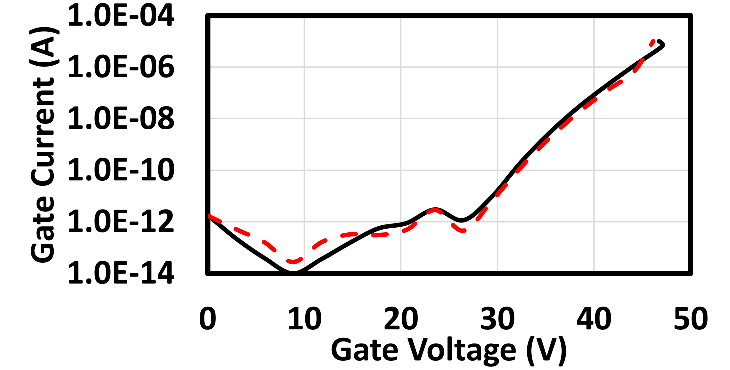
6.5kV MOSFET with One-Channel layout



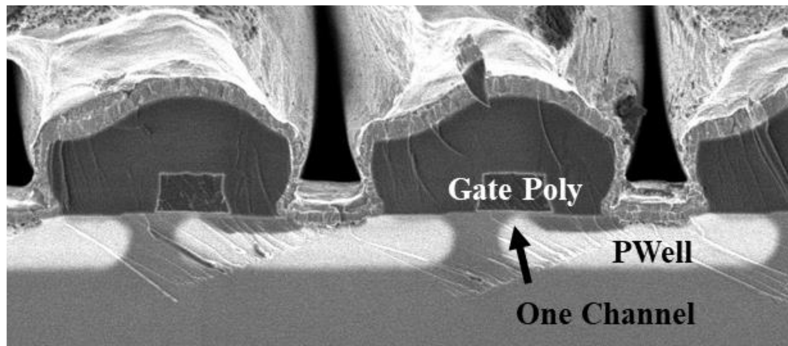
Conventional SiC MOSFET SEM.



The effect of temperature on specific on-resistance and threshold voltage are shown for the conventional MOSFET (black solid line) and one-channel MOSFET (red dotted line).

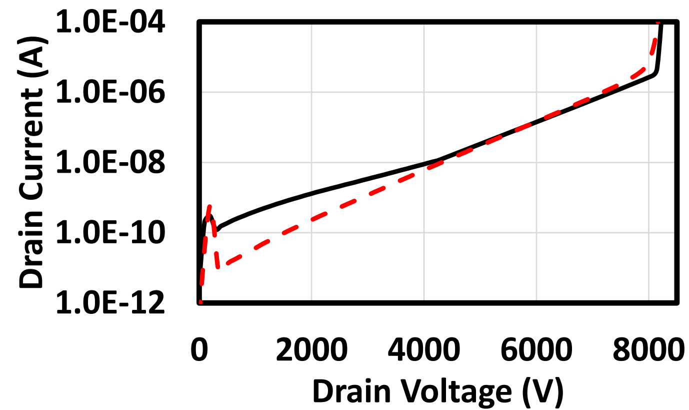


Measured I_{GSS} characteristics of the conventional MOSFET (black solid line) and one-channel MOSFET (red dotted line).

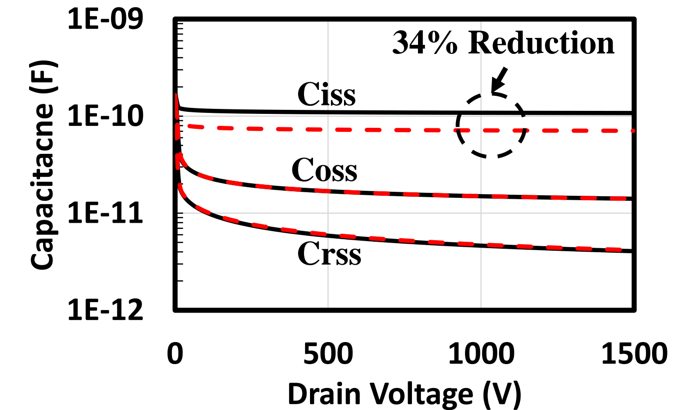


One-Channel SiC MOSFET SEM.

Fabricated at SiCamore, 2023



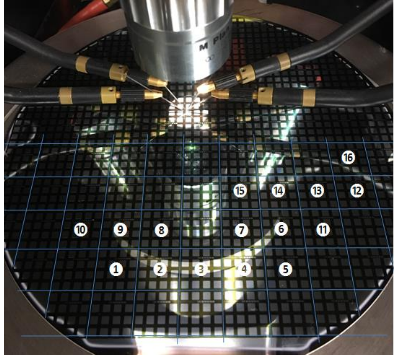
Measured forward blocking behaviors for the conventional MOSFET (black solid line) and one-channel MOSFET (red dotted line).

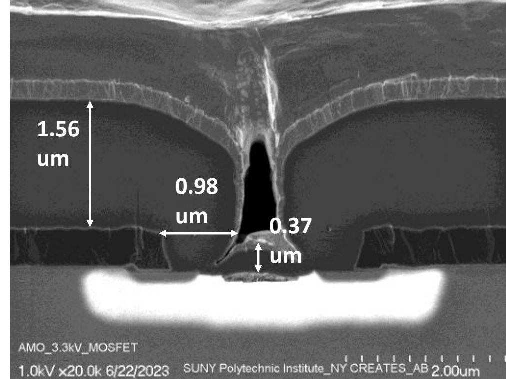


Measured capacitance curves for the conventional MOSFET (black solid line) and one-channel MOSFET (red dotted line). Measurements at a 1 MHz frequency and with a 0 V gate-source voltage.

J. Lynch, et al., "A Novel 6.5 kV 4H-SiC MOSFET with a One-Channel Layout," 2024 IEEE 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Bremen, Germany, 2024.

Recent work on 3.3kV Devices





2018

3.3kV, 4.5kV rated SiC Diodes

Fabricated at X-FAB

Demonstrated efficient edge termination structures: RA-JTE, MFZ-JTE, and Hybrid-JTE

2023

3.3kV rated SiC MOSFETs, JBSFETs, Ti-JBS

Fabricated at SiCamore (Bend, Oregon)

Process issue (ILD double deposited, G-S short)

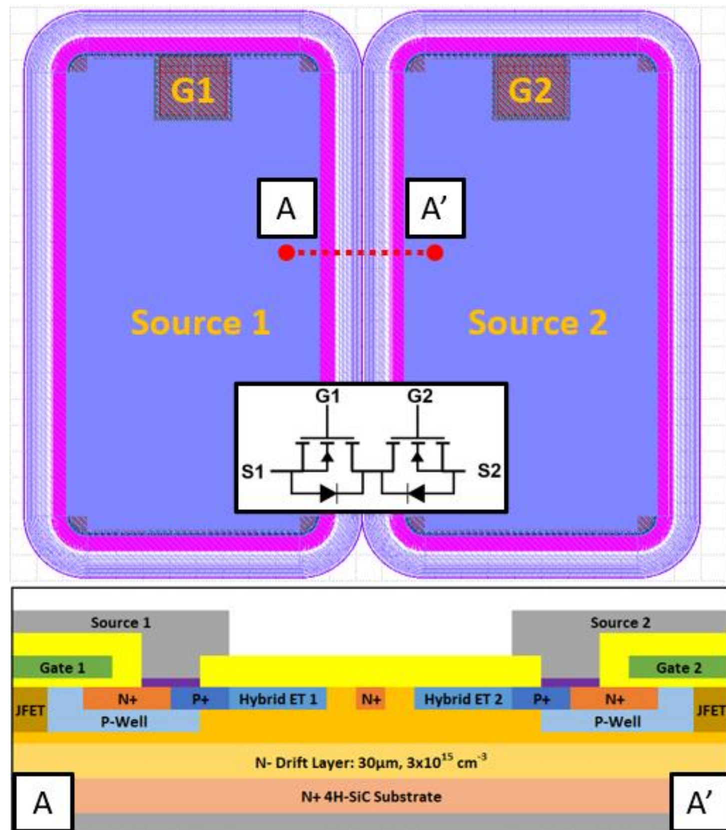
2023

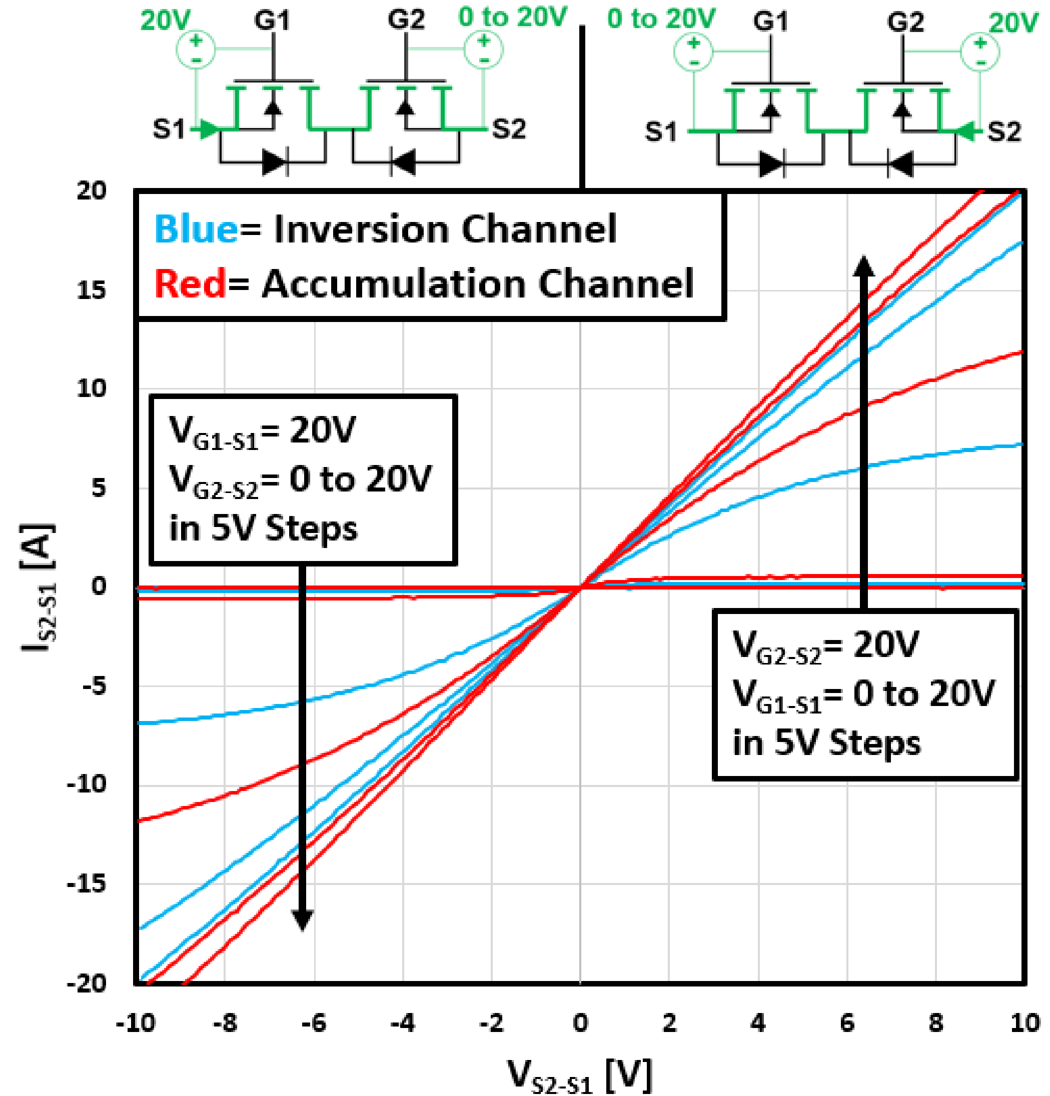
3.3kV SiC MOSFETs, BiDFETs

Fabricated at Clas-SiC (UK)

Demonstrated monolithically integrated Bi-directional switches (BiDFETs)

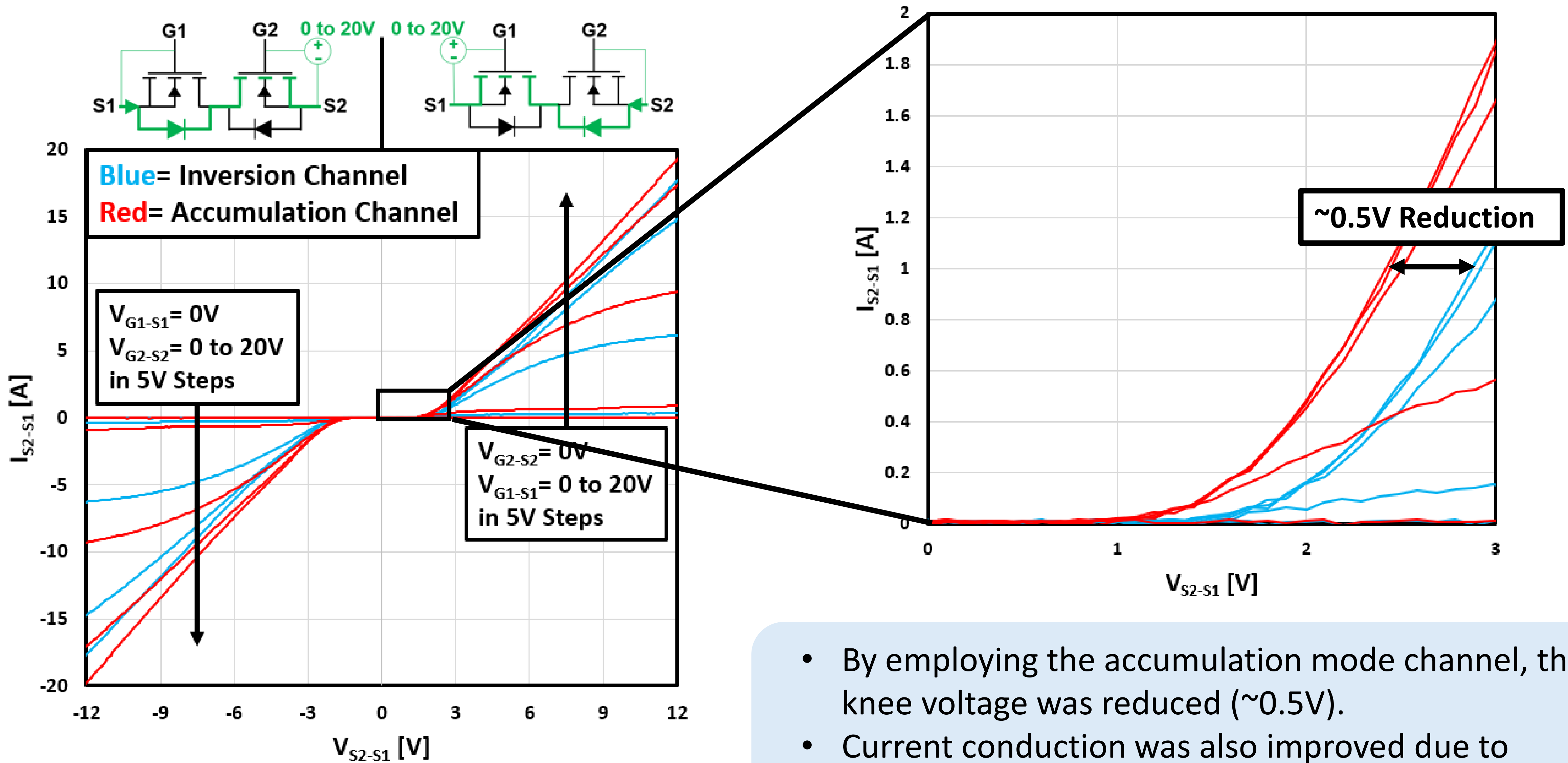
Monolithically integrated Bi-directional MOSFETs





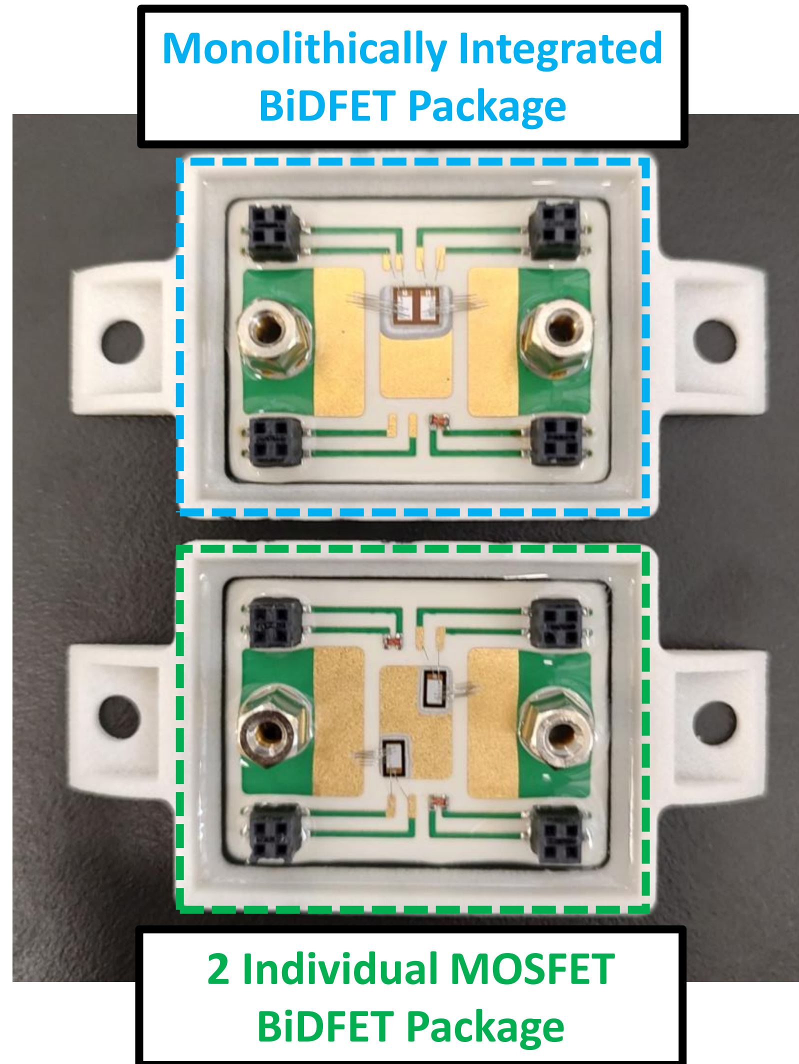
S. A. Mancini *et al.*, "Monolithically Integrated >3kV, 20A 4H-SiC BiDFET Utilizing an Accumulation Mode Channel for Improved Output Characteristics," *2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Bremen, Germany, 2024, pp. 339-342, doi: 10.1109/ISPSD59661.2024.10579613.

Monolithically integrated Bi-directional MOSFETs

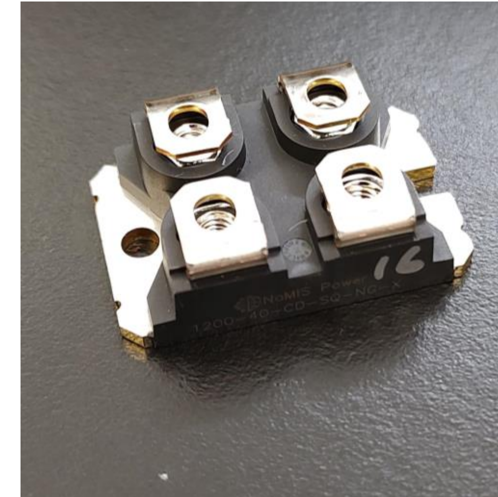


- By employing the accumulation mode channel, the knee voltage was reduced (~0.5V).
- Current conduction was also improved due to higher channel mobility.

Monolithically integrated Bi-directional MOSFETs



Both devices were packaged by NoMIS Power



SOT227 packaged by Fastech

- Being evaluated at OSU and Sandia National Lab

Lessons learned

- As the epi-layer becomes thicker, more defects/dislocations can be prevalent in the wafer.
- Bypassing body-diode operation resolve the BPD-induced degradation.
- Channel resistance is still determining factor for high voltage devices.
- Careful design of epi-stack and implant recipes are required.
- Less stringent when improving ruggedness of those high voltage devices as the increase in on-resistance.

Barriers

Fabrication facility:

- NO volume production fabrication facility offer 6.5kV or higher ;
- X-FAB will soon offer 3.3kV process service;
- GE starts their services to public users – prototyping or small volume.
- MUSiC (Multi-User SiC) fab in U of Arkansas – will be available soon.

High quality materials:

- Process yield is largely affected by epi-quality;
- Need more vendors – Coherent is the only vendor that sells thick epi-wafer with reasonable lead time

Thank you!

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