2024 Power Electronics & Energy Conversion Workshop

The Bradley Department of Electrical and Computer Engineering
College of Engineering

Blacksburg, Virginia, USA

Multidimensional power devices in WBG and UWBG semiconductors

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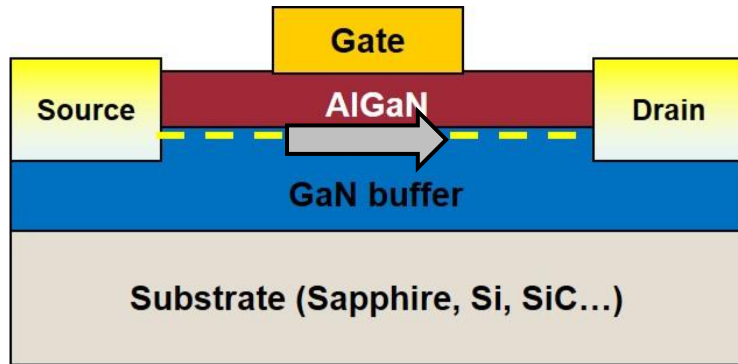
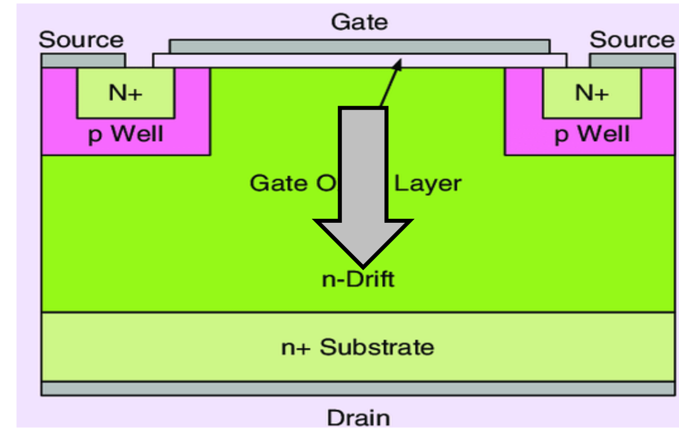
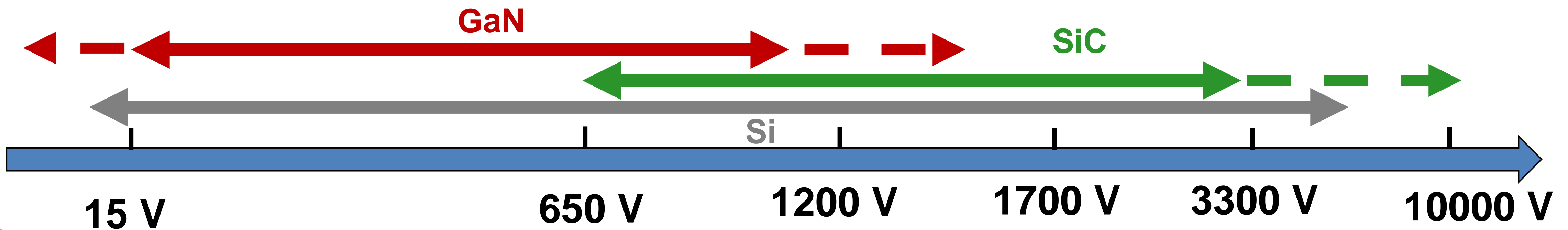
Device architectures: GaN HEMTs and SiC MOSFETs



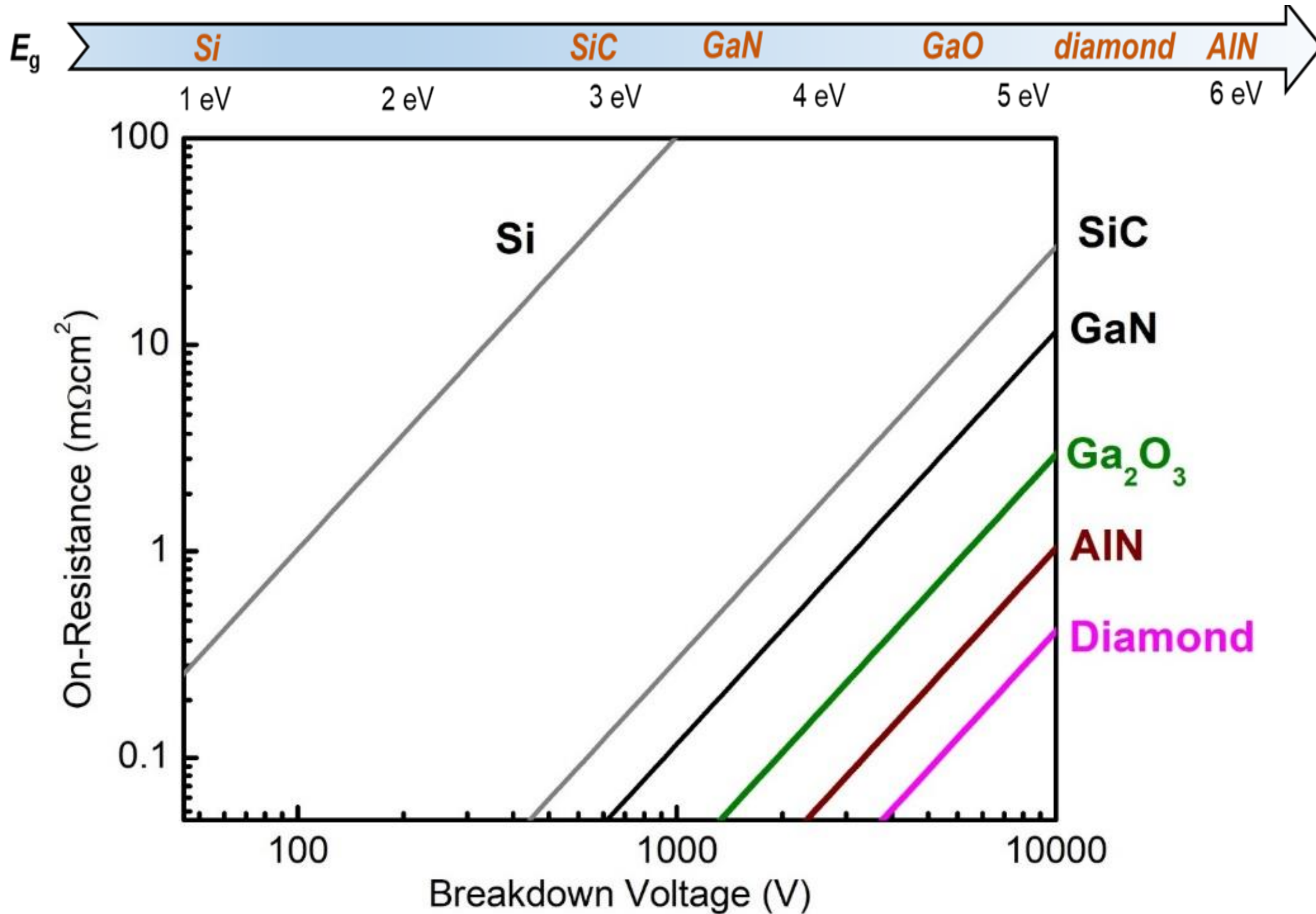


- √ 2DEG: mobility >1500 cm^2/Vs
- √ easy for IC integration
- × large chip size for high-voltage
- × thermal and E-field management
- × robustness (avalanche and short-circuit)

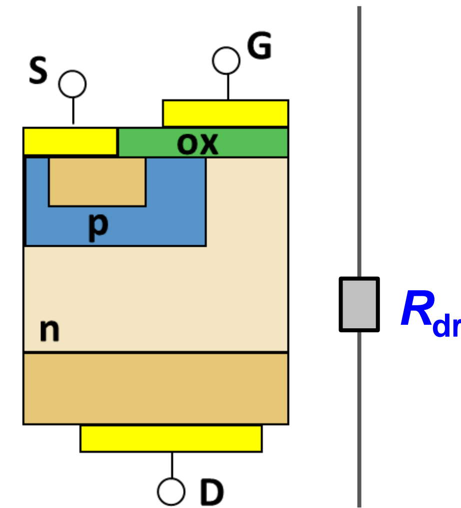
- × MOS: mobility ~100 cm^2/Vs
- × Mostly discrete
- √ high current
- √ small chip size for high-voltage
- √ easier thermal management



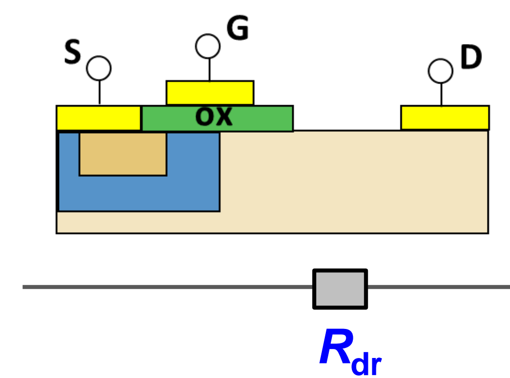
True material limits of power transistors



Vertical FET

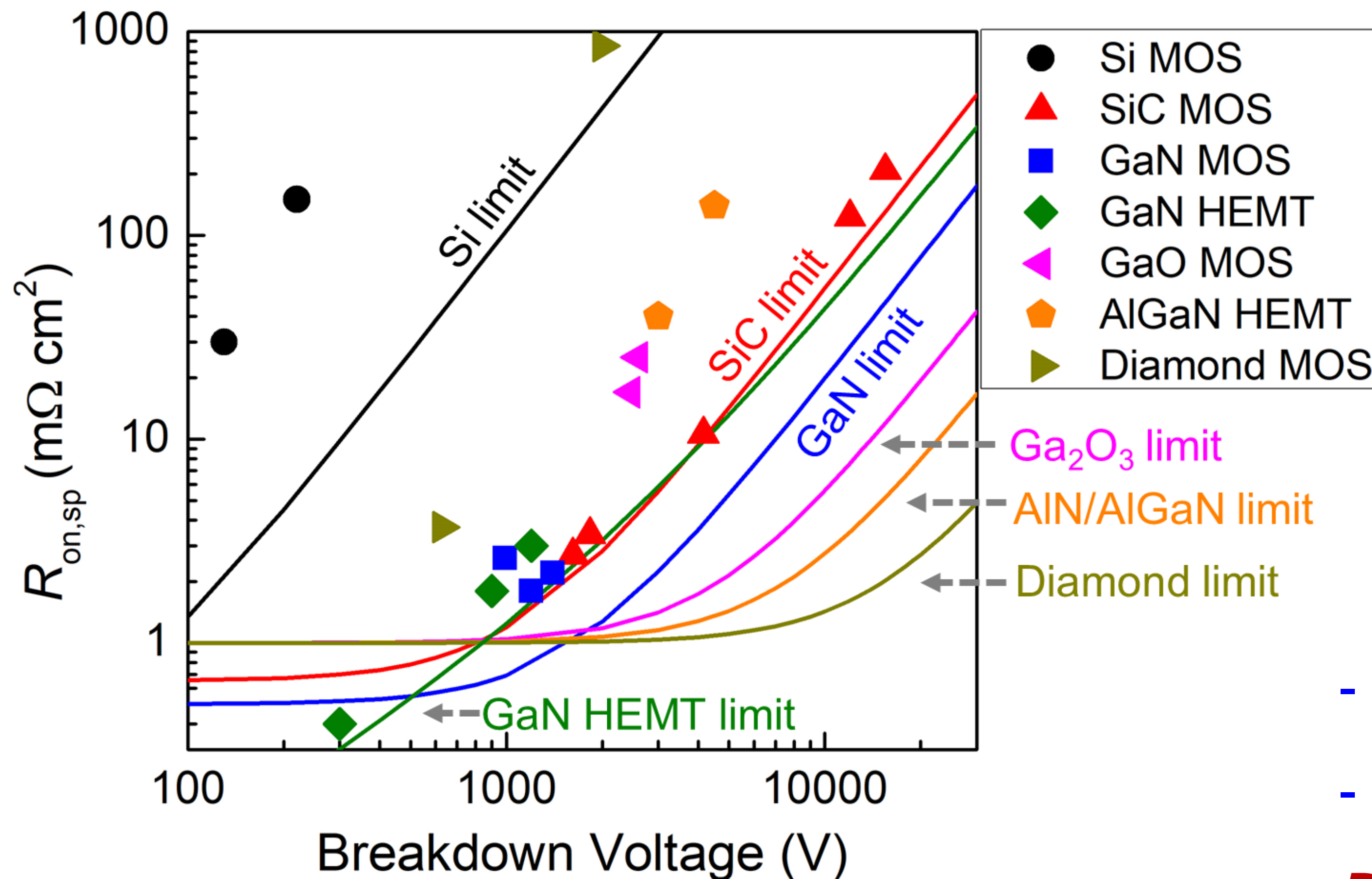


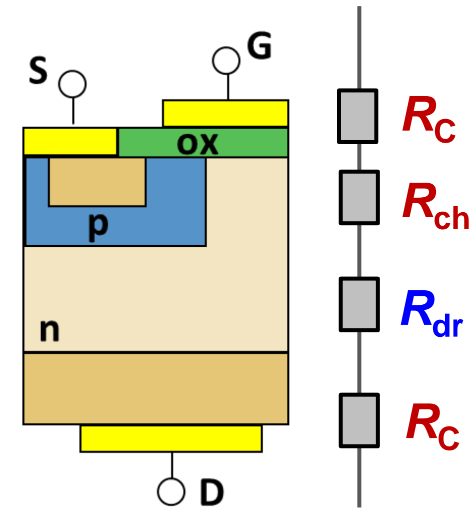
Lateral FET

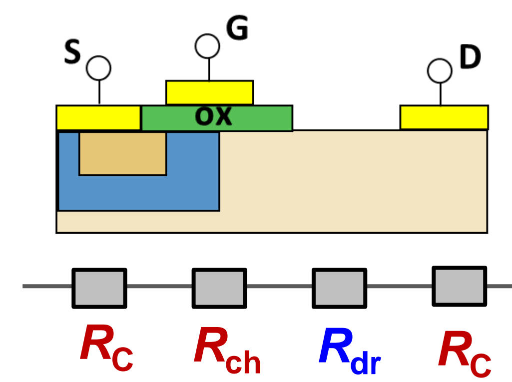


$$R_{\mathrm{on},sp} = \frac{4BV^2}{\varepsilon \mu E_C^3} \qquad R_{\mathrm{on},sp} = R_{\mathrm{on}} \cdot A$$

True material limits of power transistors





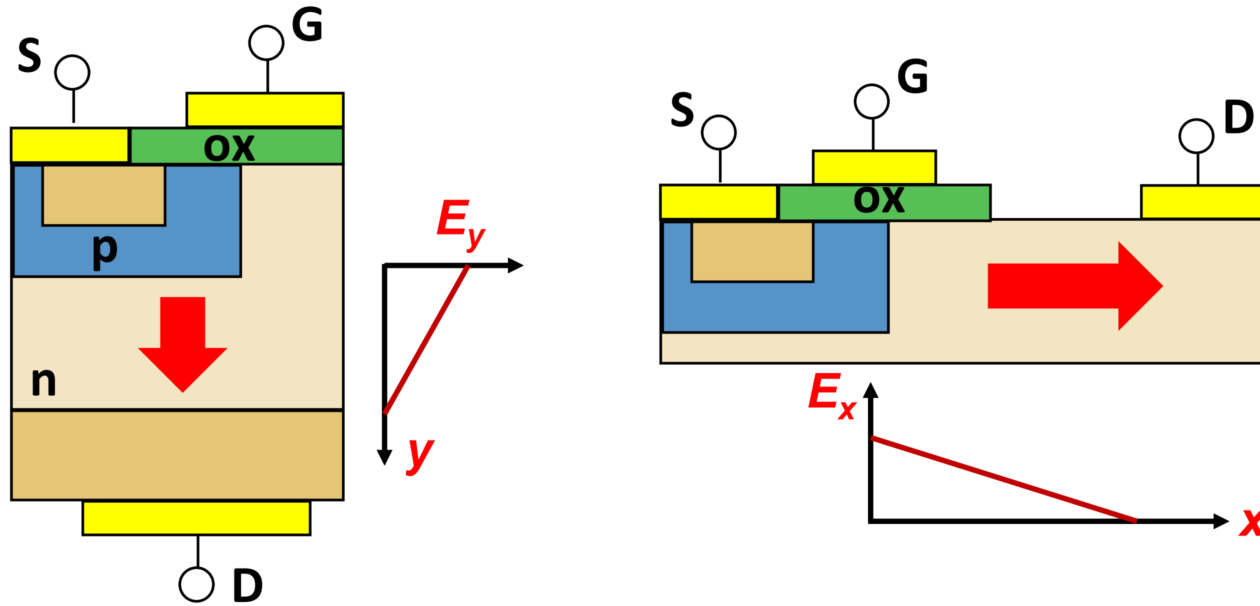


- **How to slash R_C + R_{CH}?**
- **How to reach/break material limit?**

Device architecture matters!

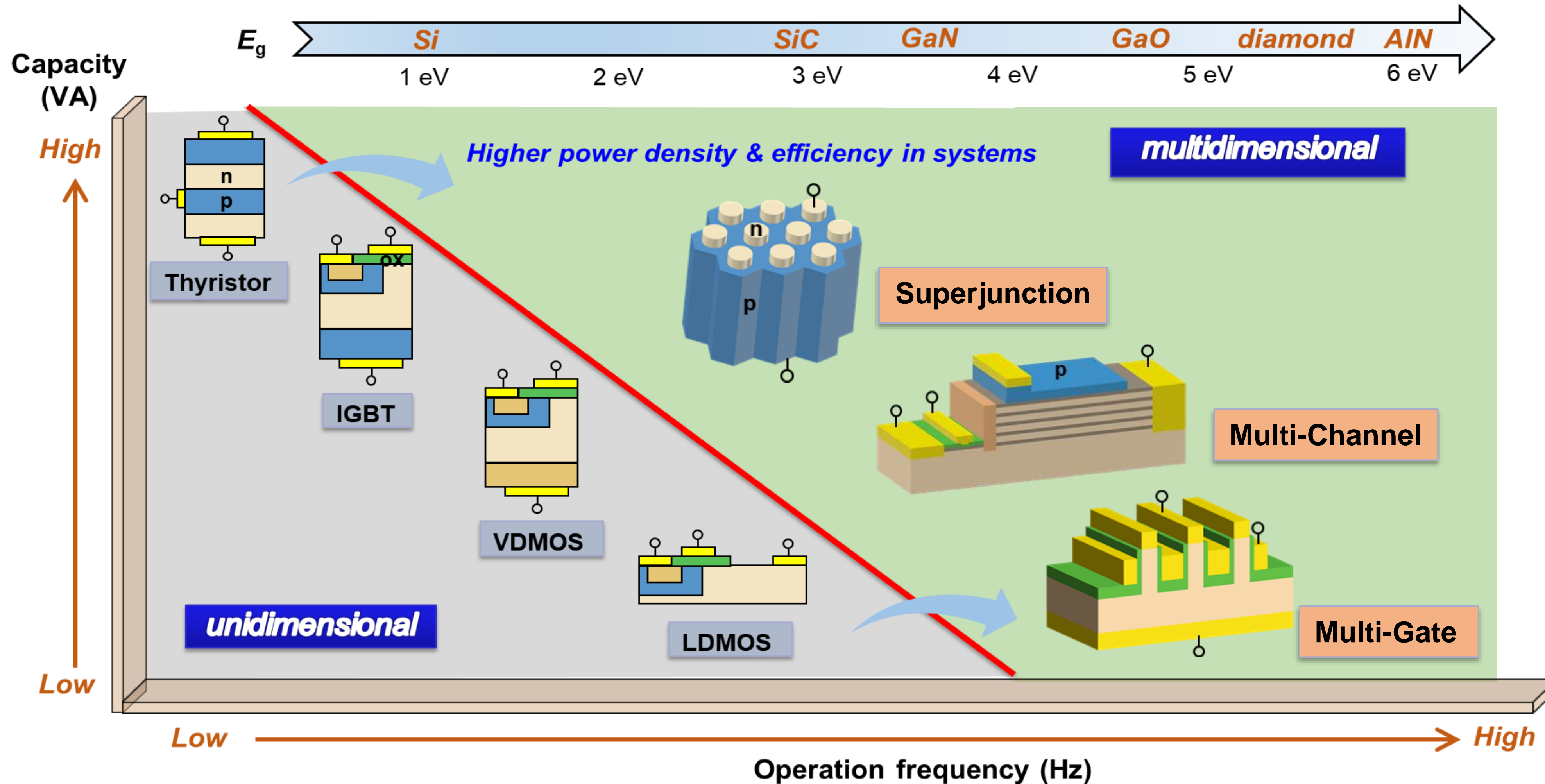
Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

Conventional power devices: 1D



- 1-D power device: voltage (field) blocking along the direction of current conduction

Multidimensional power devices



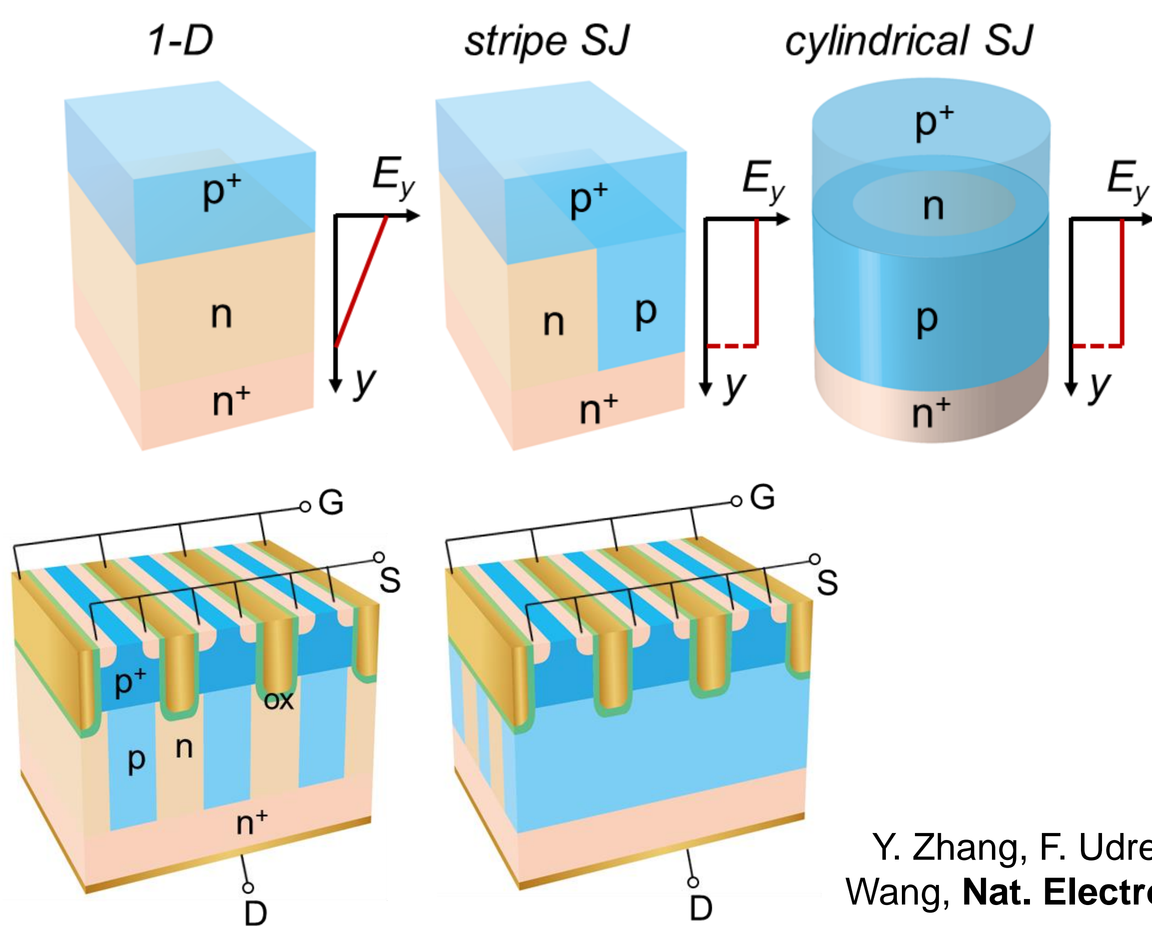
Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

- electrostatic engineering in at least one additional geometrical dimension
- break the capacity-frequency and $R_{ON,SP}$~BV trade-off

Outline

- Introduction
- Superjunction
- Multi-channel
- Multi-gate
- Performance limits and scaling law
- Summary

Superjunction: multidimensional E-field engineering



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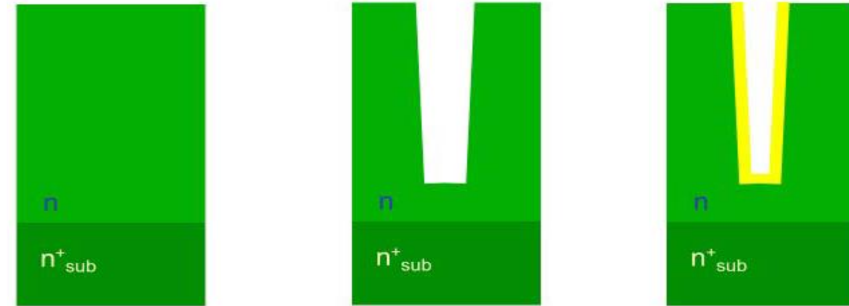
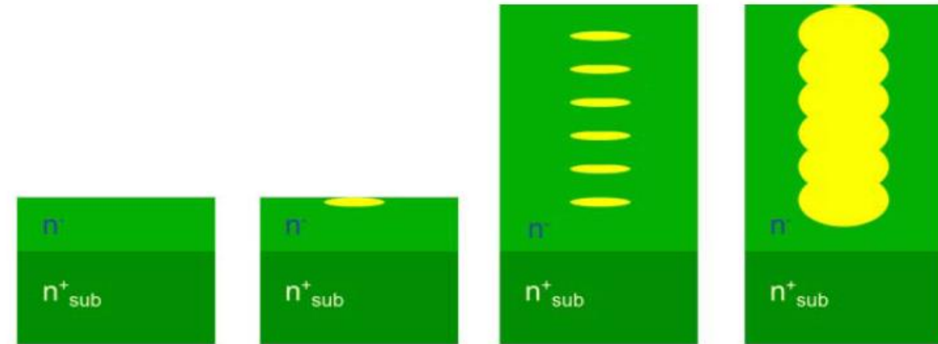
Trench-filling regrowth



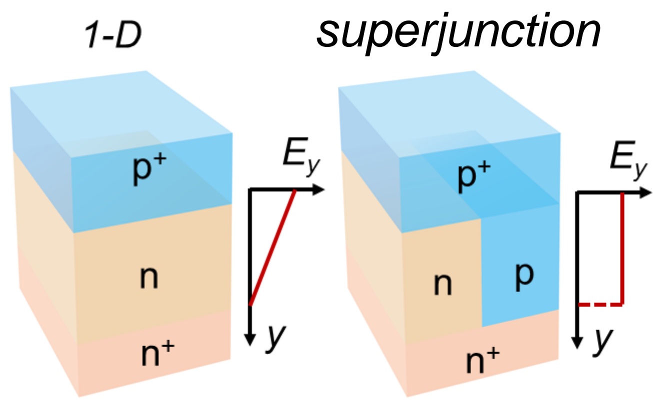
Multi-epitaxy + ion implantation

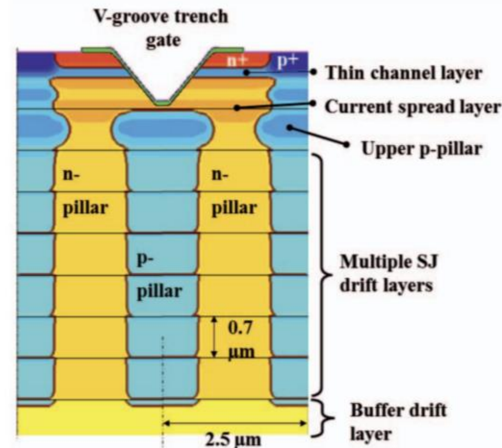


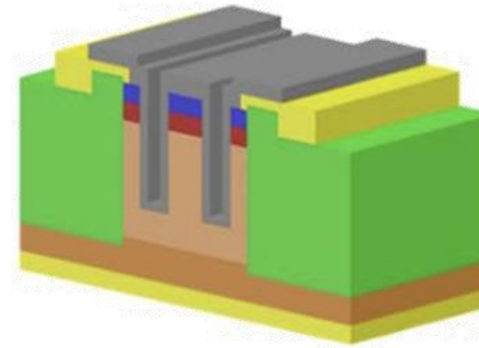
F. Udrea, G. Deboy, T. Fujihira, **T-ED** 17

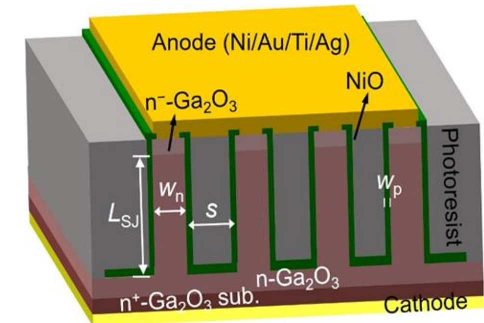
- Superjunction: alternative p- and n-type pillars with precise charge balance
- Uniform E-field along the voltage blocking direction; much higher doping than 1D devices
- Break 1-D limit of $R_{ON,SP}$ ~ BV trade-off and enable a linear dependence

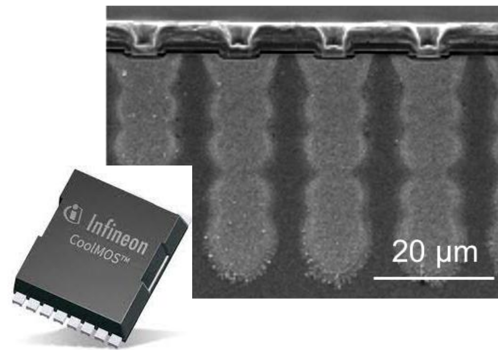
Vertical superjunction: from Si to WBG and UWBG

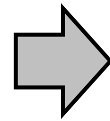


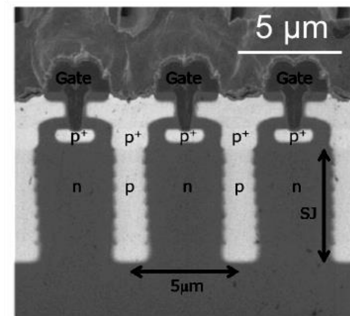


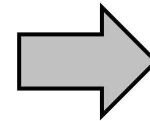


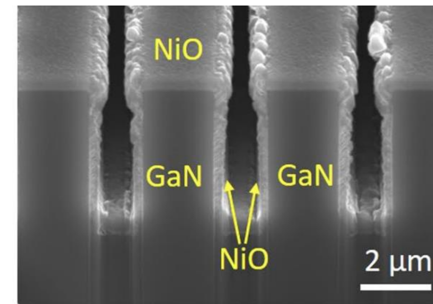


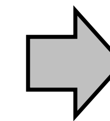


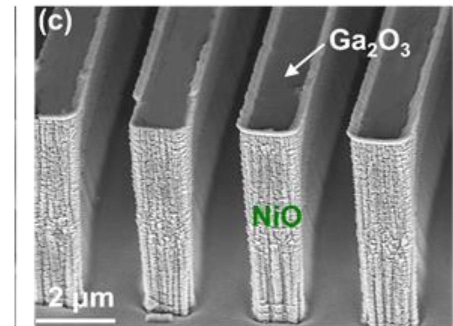












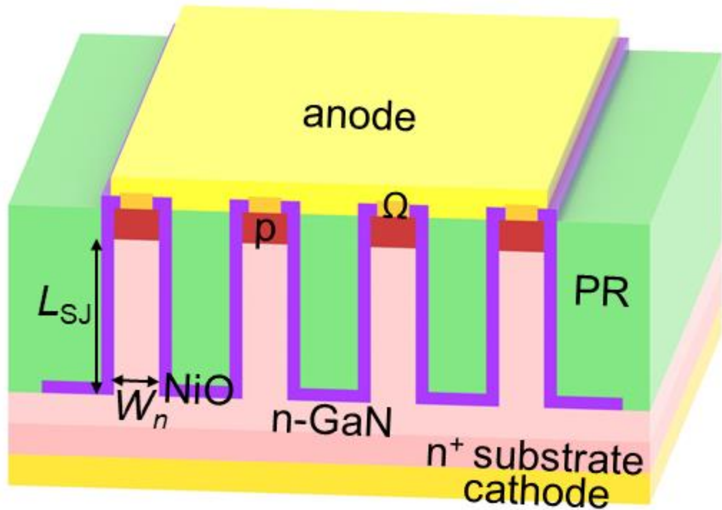
Si superjuction
commercial since 1998
~$1billion market

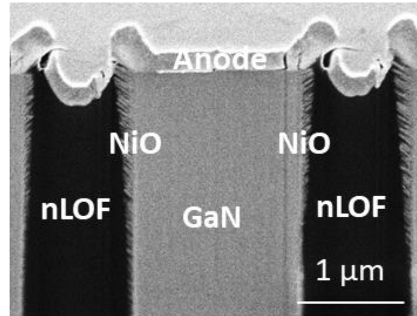
SiC superjuction
1st demo in 2016-2018
1.2kV, 0.63mΩ·cm²

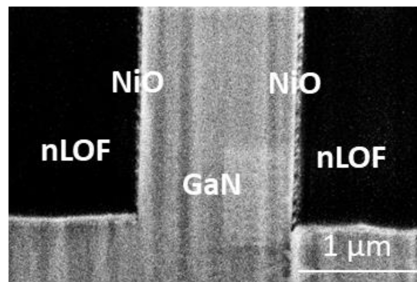
GaN superjuction
1st demo in 2022
1.1kV, 0.3mΩ·cm²

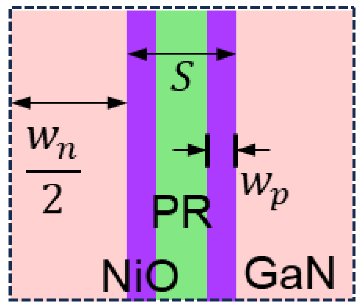
Ga_2O_3 superjuction
1st demo in 2023
2kV, 0.7mΩ·cm²

Superjunction in GaN: homogenous -> heterogeneous





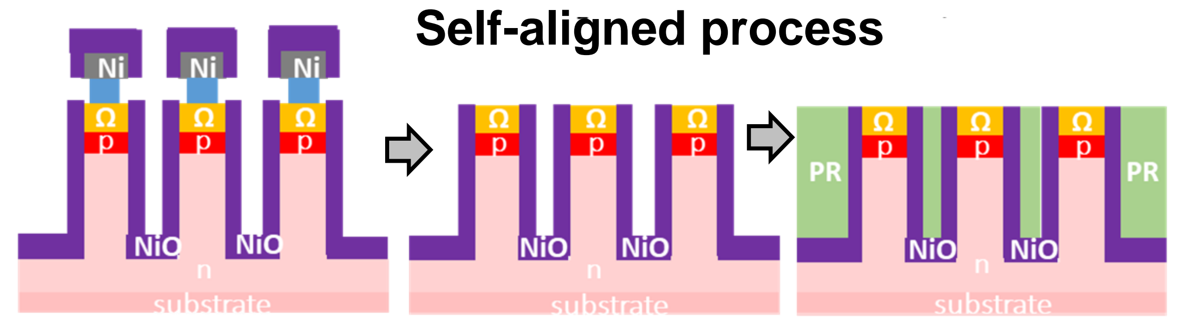




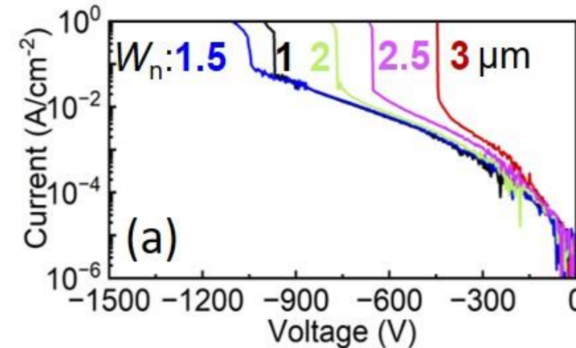
Charge balance

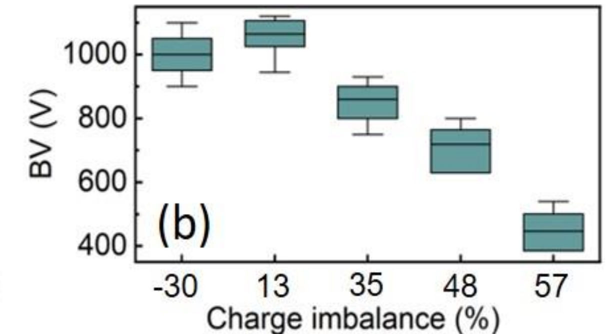
$$w_p N_A = N_D w_n/2$$

Self-aligned process



BV modulated by charge balance (SJ signature)

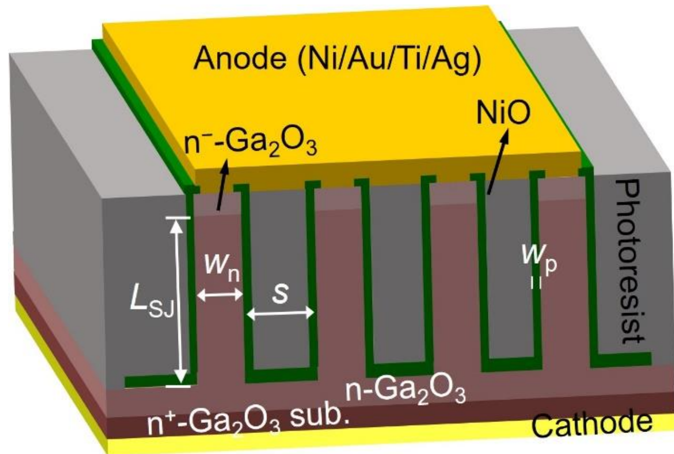


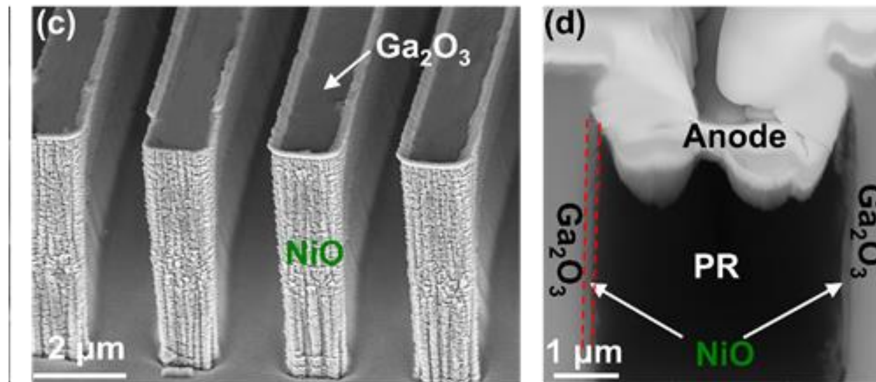


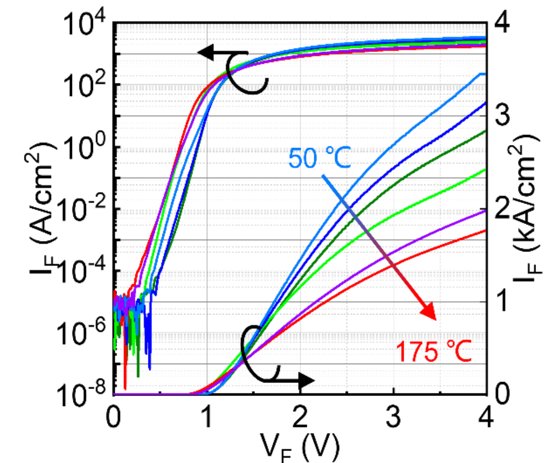
M. Xiao, Y. Zhang* *et al.*, **IEDM** 35.6, 2022
Y. Ma, Y. Zhang* *et al.*, **EDL**, 45, 1, Jan. 2024

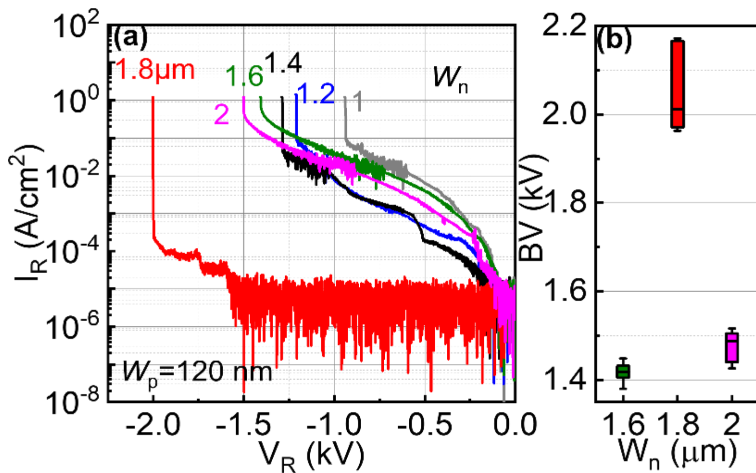
- NiO (E_g: 3.4~4 eV) sputtered on GaN sidewall, N_A tuned by O_2/Ar ratio in NiO sputtering
- Drift region doped 10X higher than 1D devices -> ultra-low $R_{DR,SP}$ ~ 0.15 mΩ·cm^2
- $R_{DR,SP}$~ BV break the 1-D GaN limit

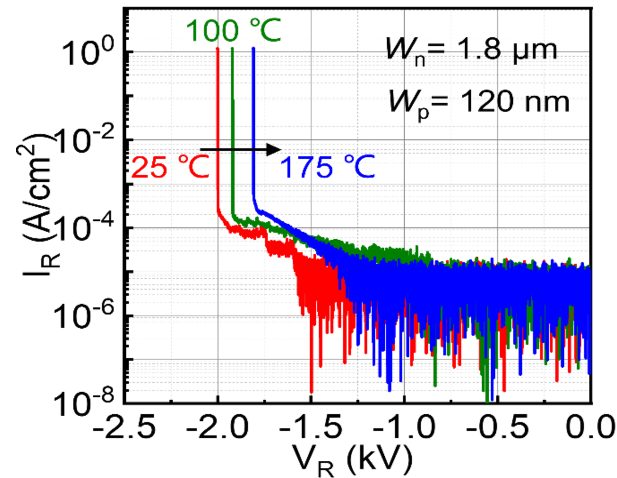
Heterogenous superjunction in UWBG Ga_2O_3

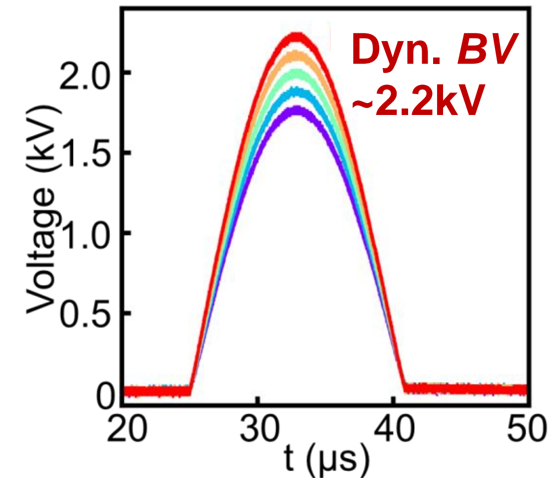








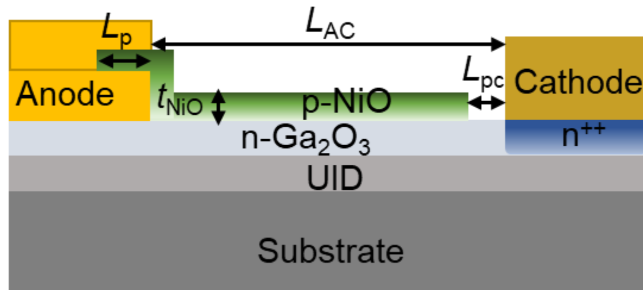


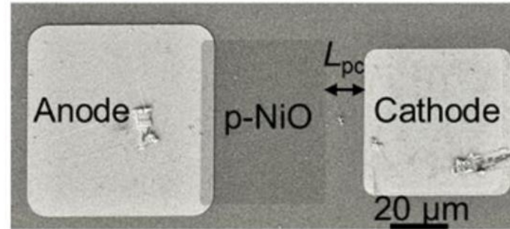


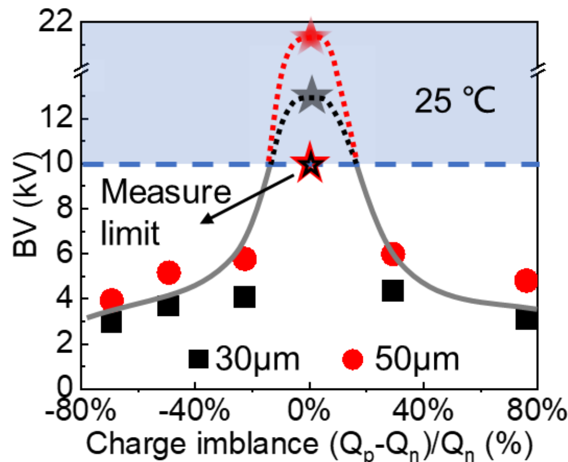
Y. Qin, Y. Zhang*, *et al.*, **IEDM 23**

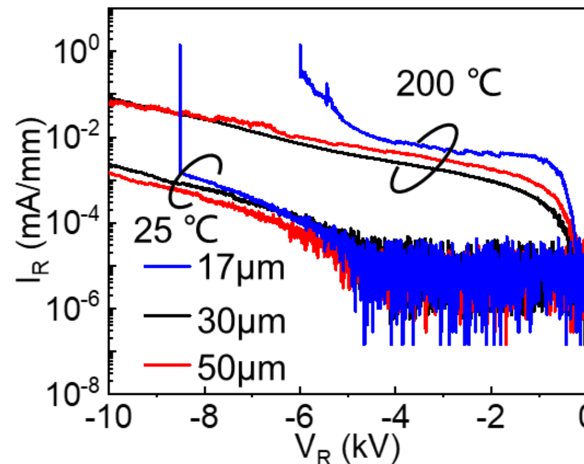
- 2kV, 0.7 mΩ·cm² Ga_2O_3/NiO SJ diode, record FOM in Schottky diodes
- Hetero-superjunction functions under high temperatures and dynamic switching

Lateral superjunction (charge-balance RESURF): 10kV Ga_2O_3 device









Device	Ave. E-field (MV/cm)
Ga_2O_3 RESURF SBD	**4.7**
Ga_2O_3 SBD	1.1
AlGaO/NiO PND	0.5
Ga_2O_3 MOSFET	1-1.4
GaN SBD	0.94
GaN HEMT	1.1
AlGaN HEMT	1.1
Diamond SBD	0.57

- 10 kV Ga_2O_3 SBD operational at 200 °C
- Primitive superjunction: BV shows strong modulation by charge balance
- Record high average E-field in lateral kilovolts devices

Y. Qin, Y. Zhang* *et al.*, **EDL**, 44, 8, Aug. 2023;
Y. Ma, Y. Qin, M. Porter, Y. Zhang* *et al.*, **Adv. Electron. Mater**. 2023.

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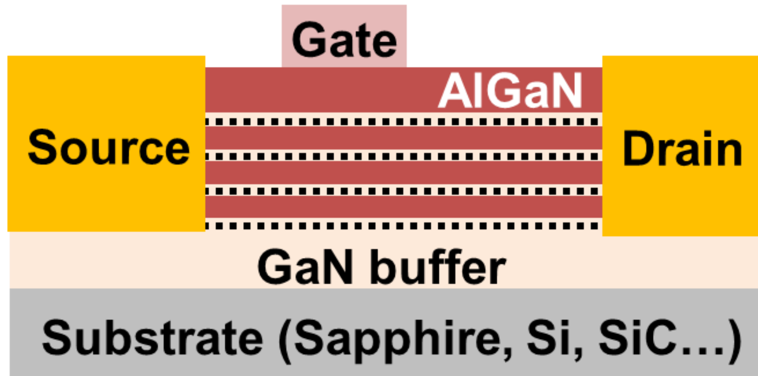
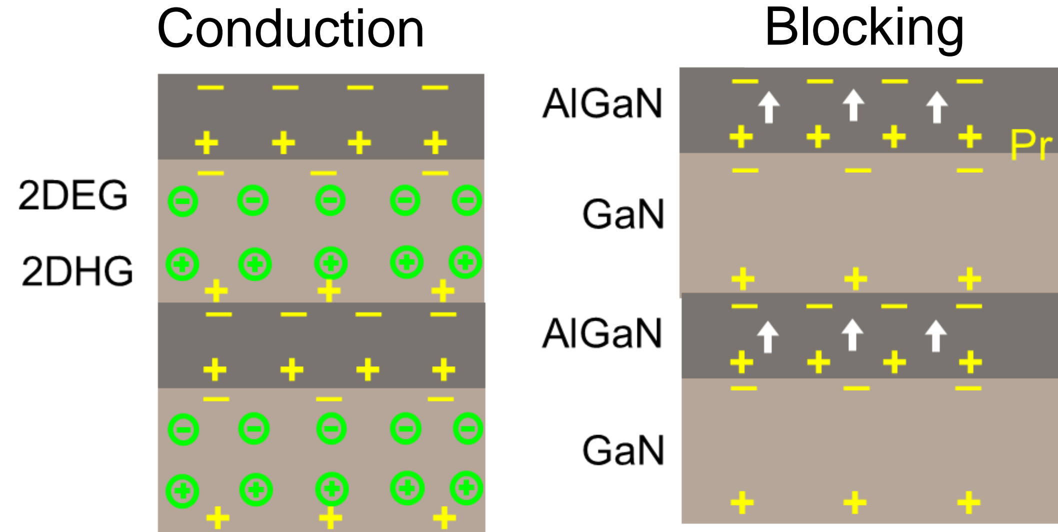
Multi-channel: lateral polarization superjunction





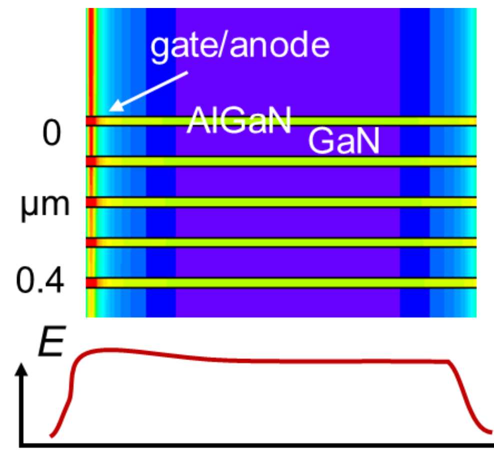
√ High current capability

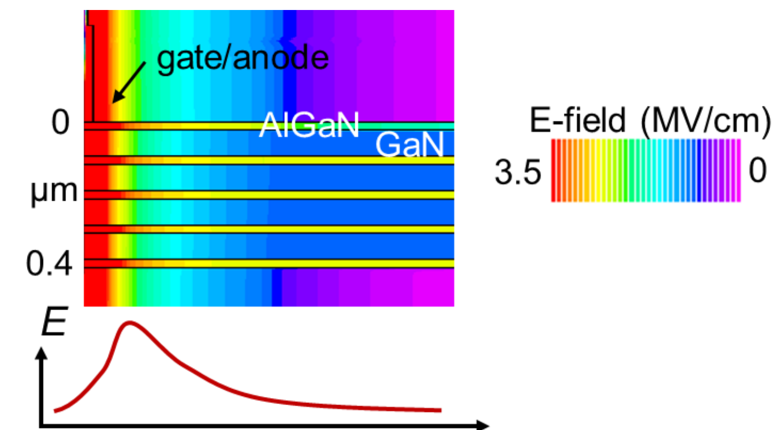
√ Low R_{on} for HV

√ Ideally, a natural superjunction

New challenges:

- **(non-ideal) E-field management**
- **E-mode gate**



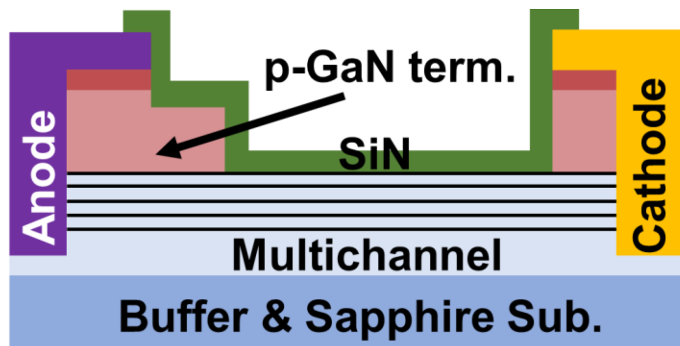


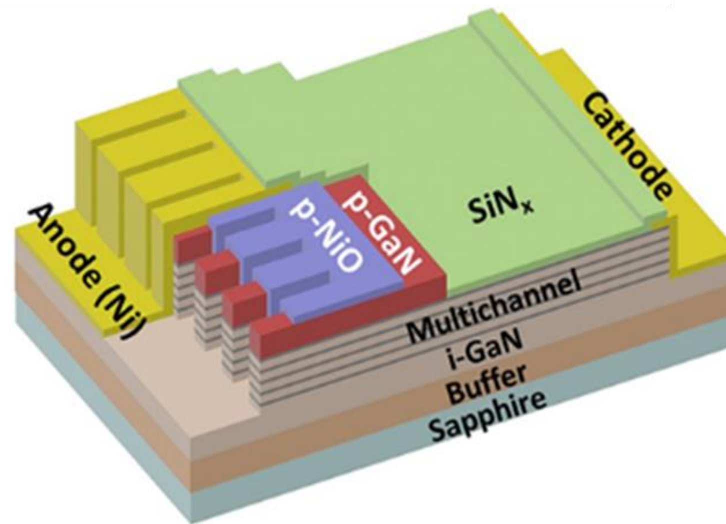
Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

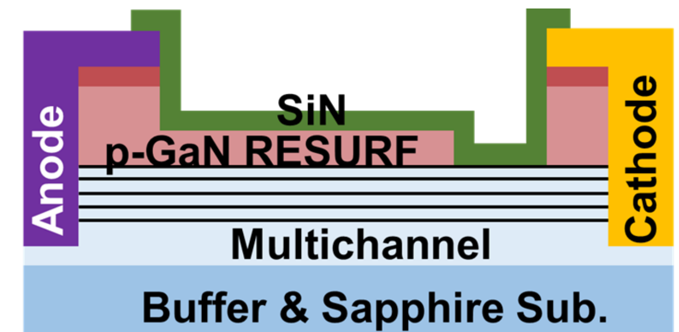
10-kV GaN multi-channel diode beyond SiC limit

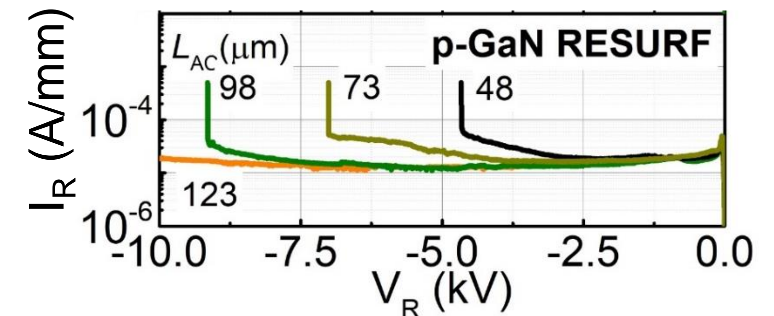
- 4-inch wafer, five 2DEG channels, R_{SH}: 120 Ω/sq
- Gen#1: P-GaN term.: no diel. interface, hole injection, foundry process -> BV over 3.3 kV
- Gen#2: 3D p-n junction wrapping around multi-2DEG fins -> 1.5 A, 5.2 kV, 13.5 mΩ·cm^2
- Gen#3: p-GaN charge balance with multi-channel ('superjunction')

  BV~11 kV, 39 mΩ·cm^2 (2.5X lower than 10 kV SiC diodes)





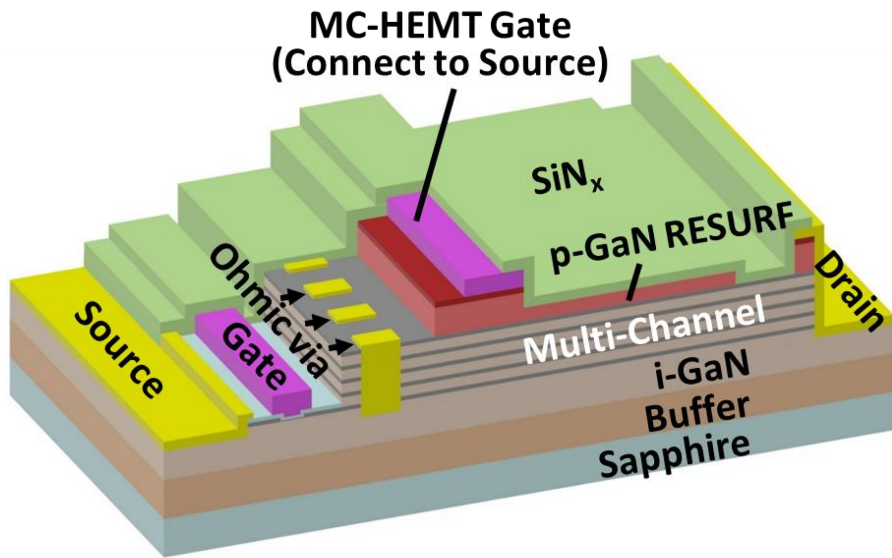


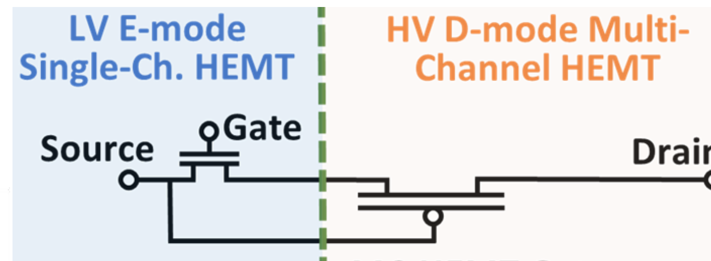


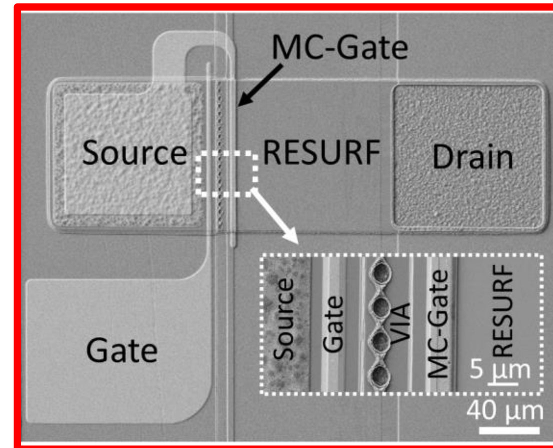
M. Xiao, Y. Zhang* *et al.*, **EDL**., 41, 8, Aug. 2020
M. Xiao, Y. Zhang* *et al.*, **IEDM**, 5.4, Dec. 2020
M. Xiao, Y. Zhang* *et al.*, **EDL**, 42, 6, 808, Jun. 2021

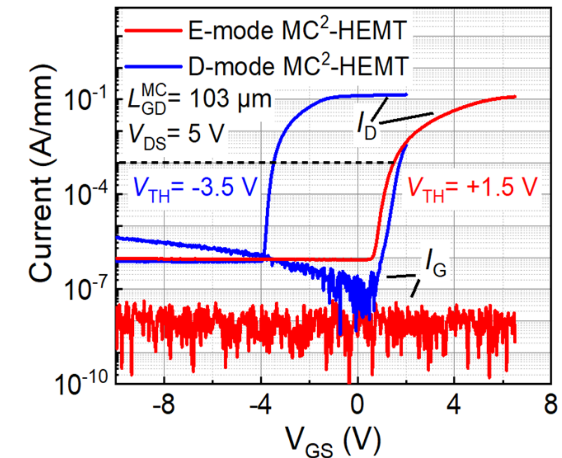
10-kV multi-channel E-mode GaN HEMTs beyond SiC limit

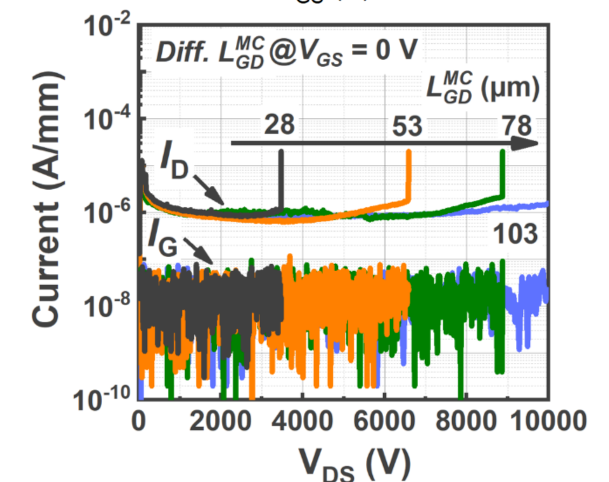
- Multi-Channel Monolithic-Cascode HEMT (MC^2-HEMT)
- R_{ON}, BV: dominated by multi-ch. HEMT; gate control by single-ch. HEMT
- V_{TH} > 1.5 V; I_{SAT} > 300 mA/mm; $R_{ON,SP}$ of 40 mΩ·cm² (>2.5x lower than SiC MOSFETs)
- Best FOM in 6.5kV+ power transistors











M. Xiao, Y. Zhang* *et al.*, **IEDM** 5.5, 2021

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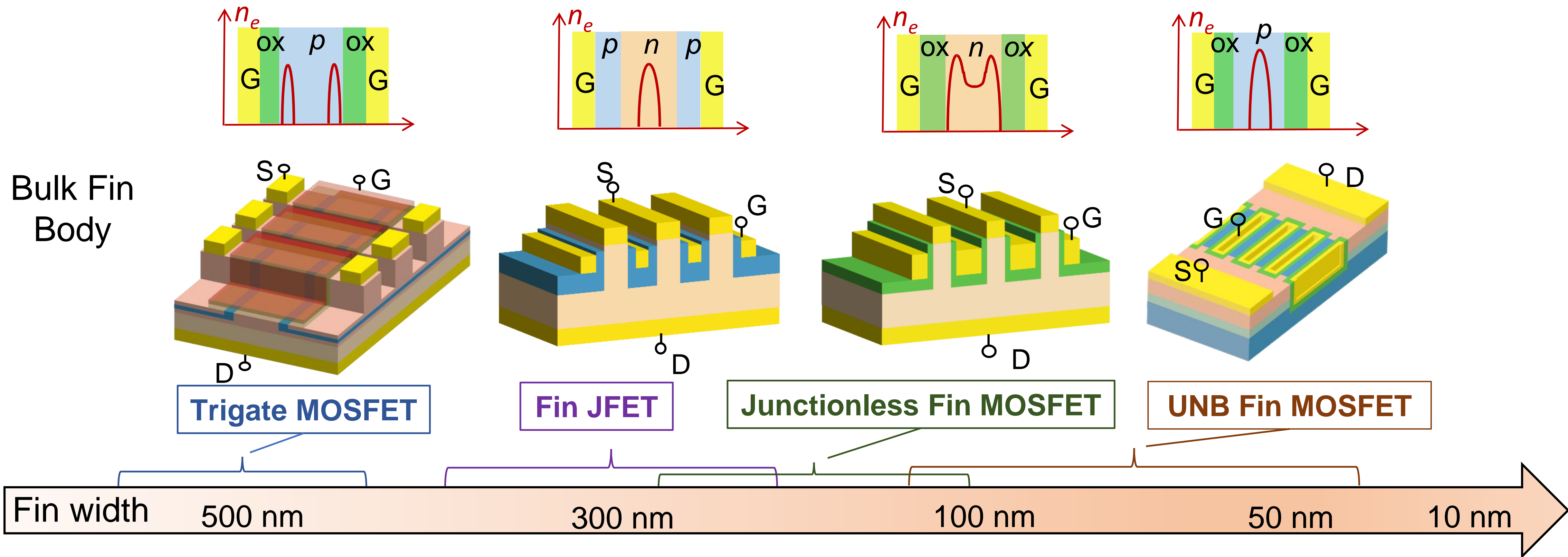
FinFET in power devices: channel innovation



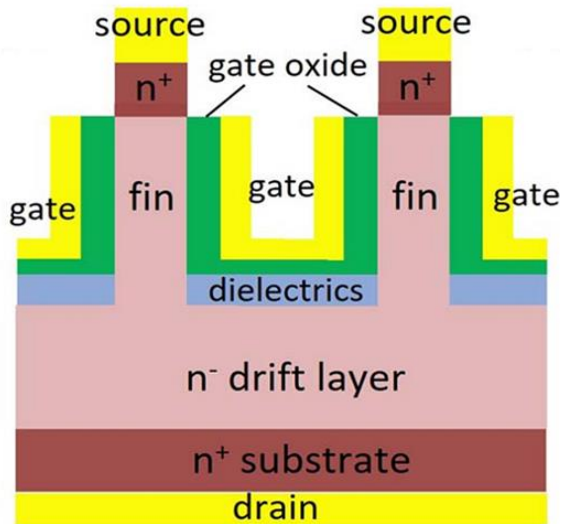
FinFET in **power**: 1) increase channel density; 2) shift carrier to high-mobility Ch.; 3) E-mode

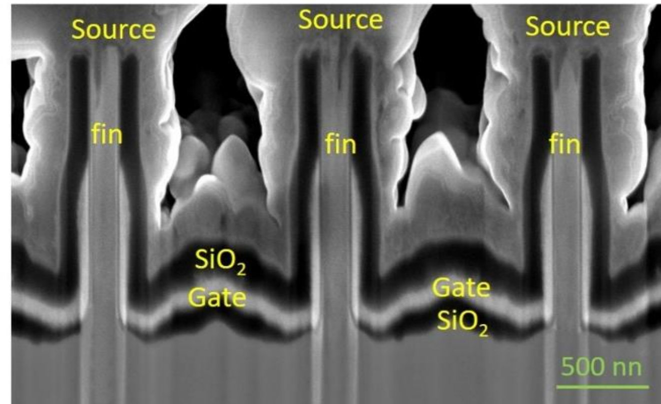
FinFET in **digital**: 1) Low SS; 2) device compactness; 3) reduce short-channel effect

Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

Vertical GaN Fin-MOSFET and Fin-JFET

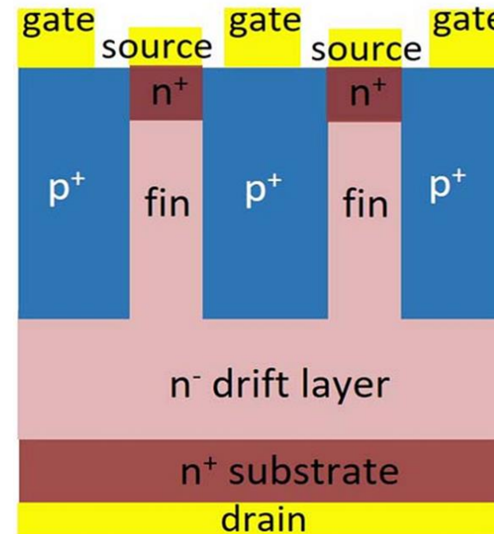
- 1.2 kV Fin-MOSFET with 200nm-wide fins
- V_{th}~1 V; $R_{on,sp}$= 1 mΩ·cm²
- 2-inch GaN-on-GaN wafer process
- Superior $R_{ON}(Q_{OSS}+Q_{rr})$ than SiC

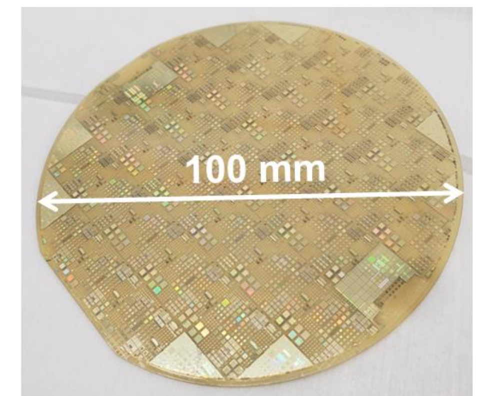




Y. Zhang, T. Palacios* *et al.*, **IEDM** 2017
Y. Zhang, T. Palacios* *et al.*, 40 (1), **EDL**, 2019

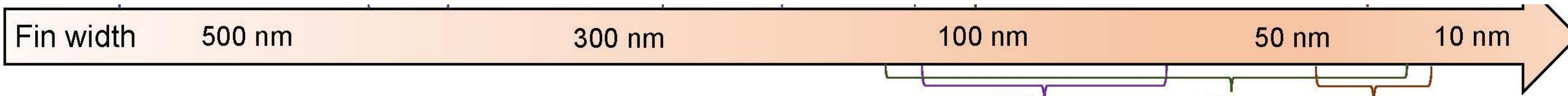
- NexGen's 1.2 kV Fin-JFET commercialization (VT characterization & application)
- $100M+ GaN-on-GaN Fab in Syracuse, NY
- 1470 V BV_{AVA}, avalanche capability, 0.82 mΩ·cm² (4-5x lower than 1.2 kV SiC MOS)



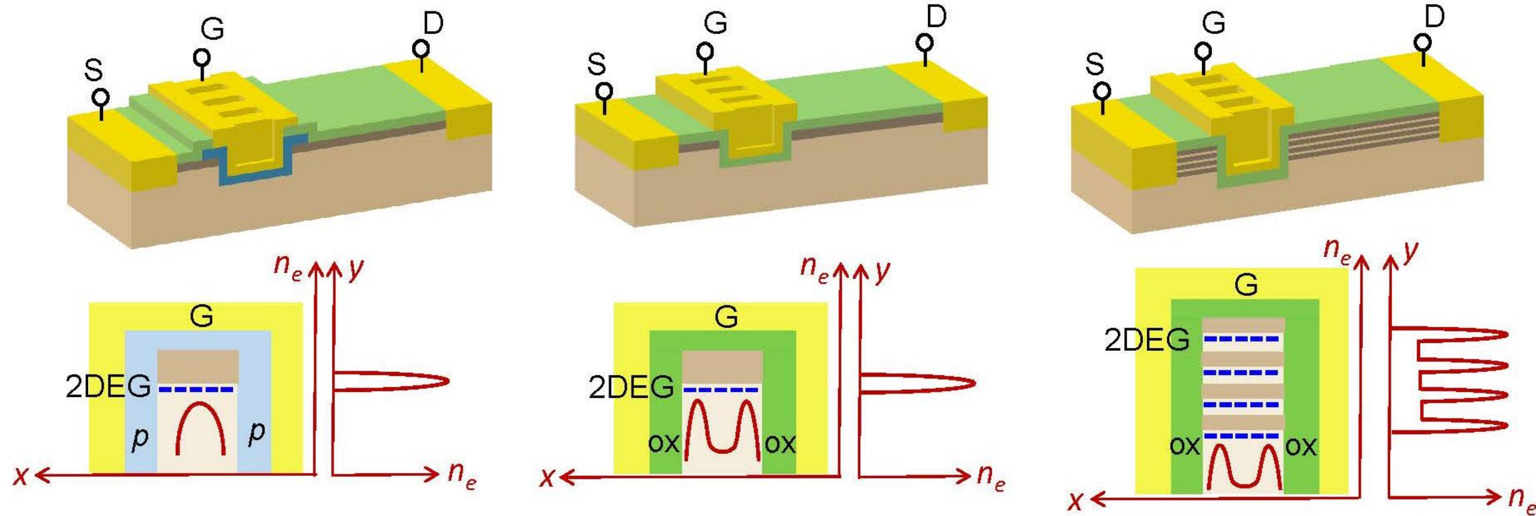


J. Liu, Y. Zhang* *et al.*, **IEDM**, 23.2, 2020; **T-ED**, 68, 2025, 2021

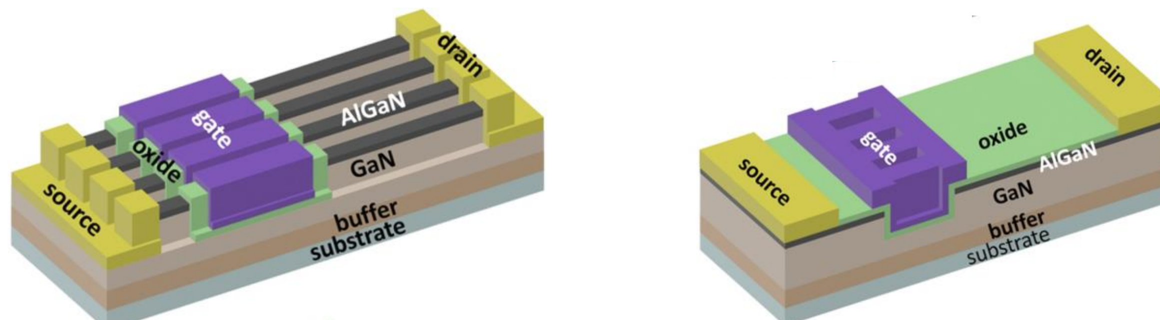
Lateral GaN Fin-HEMTs



Hetero-structural Fin Body

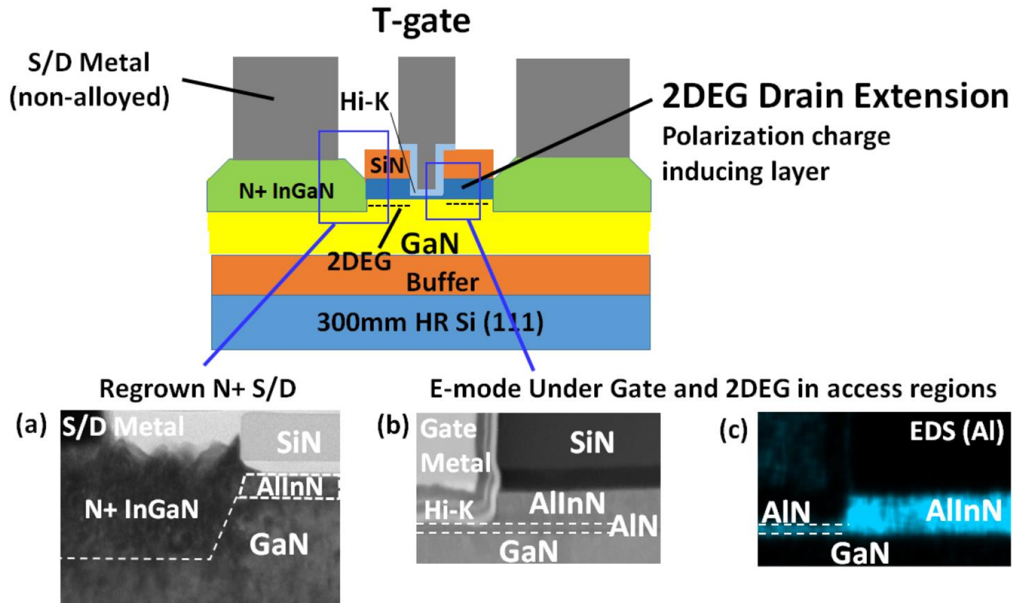


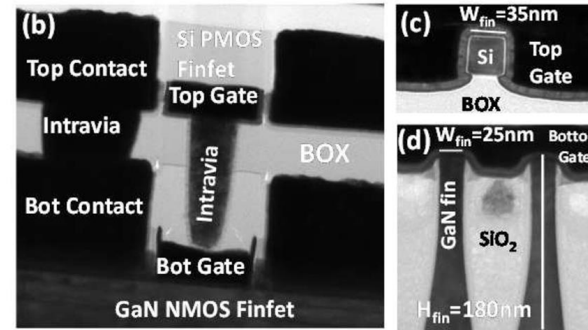
Y. Zhang, F. Udrea, H. Wang, **Nat. Electron.**, 5, 723, 2022

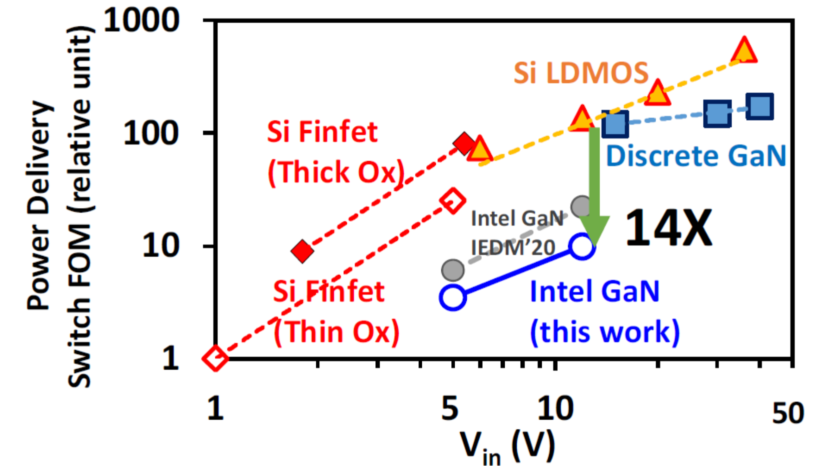


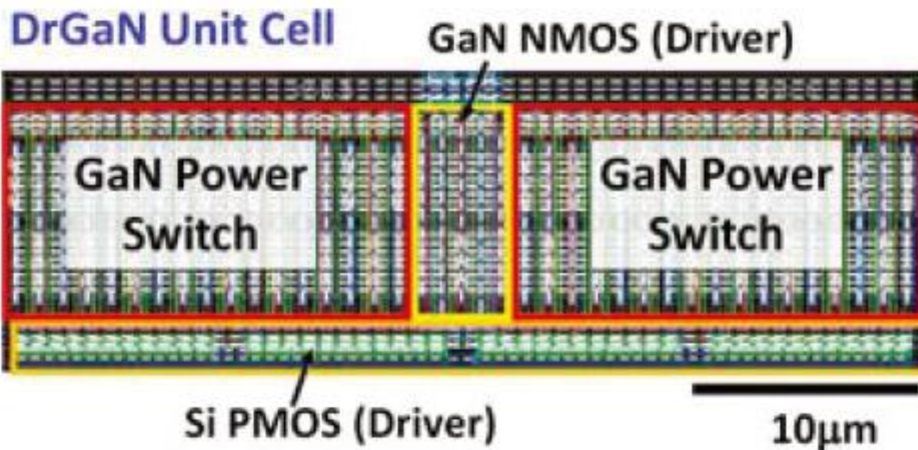
Y. Zhang, T. Palacios *et al.*, ***Semicond. Sci. Technol.***, 36, 054001 (2021)

Intel's lateral GaN Fin-HEMTs: battle Si for sub-15V power applications









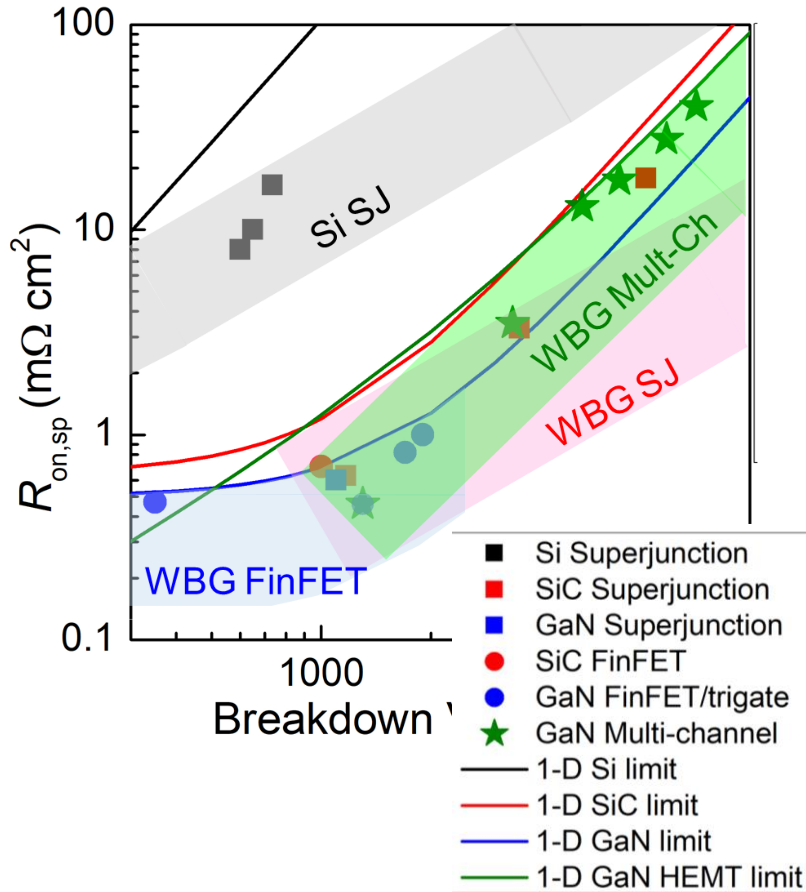
- Gate recess + regrown contact for E-mode LV HEMT
- Scaling (Fin-HEMT) enables performance advances for both GaN power and nMOS
- DrGaN: GaN power switch (GaN NMOS) + GaN-Si hybrid CMOS (GaN NMOS + Si PMOS)

Han Hui Then *et al.*, **IEDM** 15, 19, 20, 21, 22, 23

Outline

- Introduction
- Superjunction
- Multi-channel
- Multi-gate
- Performance limits and scaling law
- Summary

Multidimensional devices: new limits and new scaling laws



Drift region design	1D	2D superjunction	Multi-channel (PSJ)
Structure	S G D	n p … ←d→	N channels
Performance limit	$R_{ON,SP} = \frac{4}{\varepsilon\mu E_C^3} BV^2$	$R_{ON,SP} = \frac{4d}{\varepsilon\mu E_C^2} BV$	$R_{ON,SP} = \frac{BV^2}{NqE_C^2 n_{2D} \sum_{e,h} \mu_{2D}}$
Scaling parameter	NA	Cell pitch (d)	Channel number (N)
Scaling limit	NA	$d = \frac{50E_g}{9qE_C}$	Process and technology related
Minimum specific on-resistance	$\frac{4BV^2}{\varepsilon\mu E_C^3}$	$\frac{20E_g BV}{q\varepsilon\mu E_C^3}$	–
Material FOM	$\varepsilon\mu E_C^3$	$\varepsilon\mu E_C^{2.5}$	$E_C^2 n_{2D} \sum_{e,h} \mu_{2D}$

- Performance of multidimensional devices exceed 1D SiC and GaN limits
- Allow geometrical scaling in power devices (limit: line -> band)
- Baliga's FOM is no longer suitable for benchmarking multidimensional power devices

Y. Zhang, F. Udrea, H. Wang, **Nature Electronics**, 5, 723, Nov. 2022

Summary

- **Multidimensional architectures improve power device performance by multidimensional electrostatic engineering, which is material agnostic**
- **Rewrite performance limits and enable scaling laws**
- **Superjunction**
  - Fast development in SiC by multiple fabrication methods
  - Initial demonstrations in GaN and Ga_2O_3 breaking 1-D limits
- **Multi-channel**
  - Ideal undoped multi-channel: natural polarization superjunction
  - A new platform for high-voltage lateral devices (e.g., 10 kV GaN)
- **Multi-gate: FinFET and tri-gate**
  - Diverse form factors; significant reduction of channel resistance
  - Expand application space of WBG devices (e.g., ultra-low voltage)