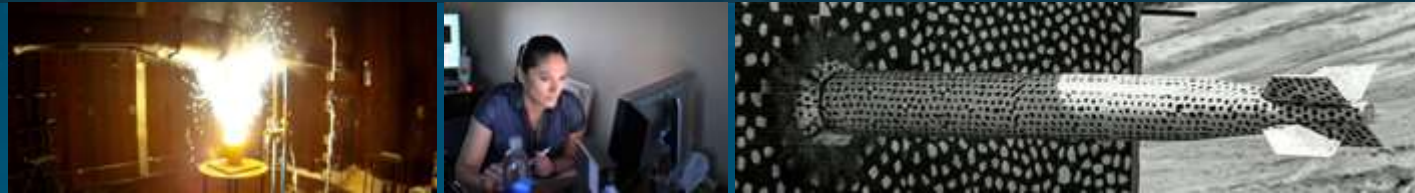


# Technical issues arising from distributed energy resource interconnections



SAND2021-6860 0

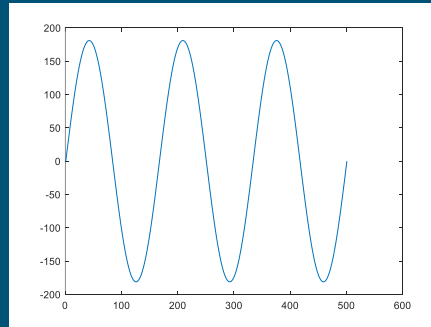
Michael Ropp, Ph.D., P.E.

## Important ones for inverter-based resources (IBRs)\*:

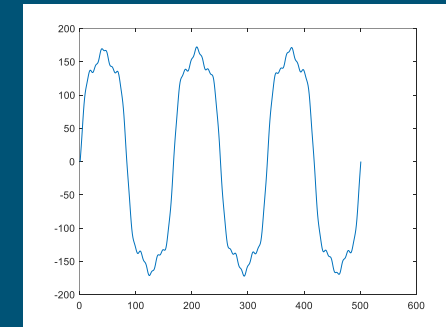
- ❑ Abnormal voltages
  - ❑ Steady-state: the IBR pushes out too much power and drives the voltage up too high
  - ❑ Transient: during certain conditions like system startup/shutdown or certain short-circuit conditions, IBRs *can* cause high or low voltages on the circuit

❑ Thermal loading—don't want IBR to push out so much power that lines overheat

❑ Power quality: want this



and not this



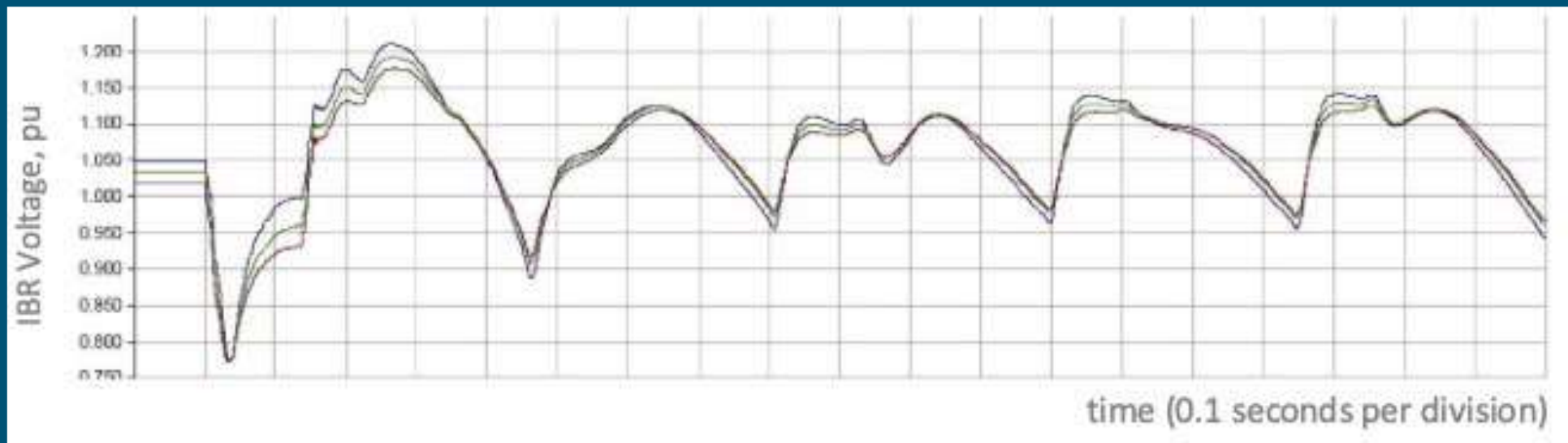
- ❑ Protection coordination—IBRs can't mess up system protection
- ❑ Unintentional islanding—IBRs need to not energize an unintentional island

\*Rotating DERs are handled differently.

## Potential technical issues at the transmission level



- ❑ Impacts of large fleets of IBRs on the dynamics of the bulk system
- ❑ Impacts on system protection
- ❑ Potential for instability
  - ❑ IBRs adversely interacting with each other
  - ❑ “Weak system” issues or resonances





Lots of work in this area at the moment (much of it at Sandia).

Standards: IEEE P1547.3 is being drafted now



Computer simulation tools are available that allow us to study the circuit/situation and check for these issues.

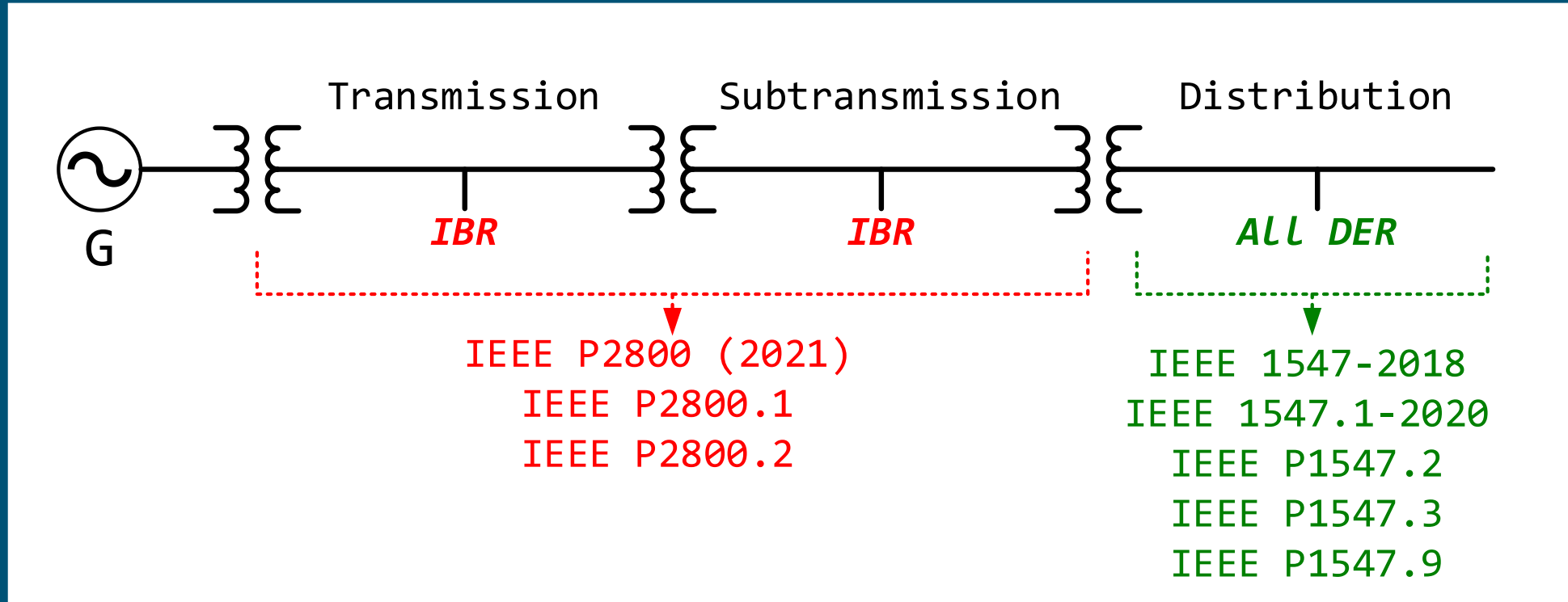
Pros: A detailed simulation model can provide a “digital twin” or “virtual laboratory” that allows experiments to be run safely and accurately, and provides detailed impacts of the DER on the proposed host circuit. *Provides reliable, quantitative answers.*

Cons: detailed studies can be costly (depending on the DER, system and issue to be studied, anywhere from a few k\$ to many tens of k\$) and can take 2-4 months to complete.

## Faster, cheaper ways of checking for these problems



- ❑ For issues related mostly to inverters themselves (power quality, unintentional islanding, transient overvoltages): rely on inverters certified to comply with standards requirements (i.e., UL 1741 certified inverters), and on specific design requirements (i.e., use a particular type of transformer). **“Type tests”**.
- ❑ For other more system-level issues (steady-state overvoltages, thermal overloads, protection): try to rely on *screens*, simple “yes/no” thresholds. Quick, easy, cheap—but ***must be conservative to avoid compromising safety/reliability***.



Streamlining  
interconnexion

Fostering innovation  
and change

## Tools to address these challenges at the distribution level

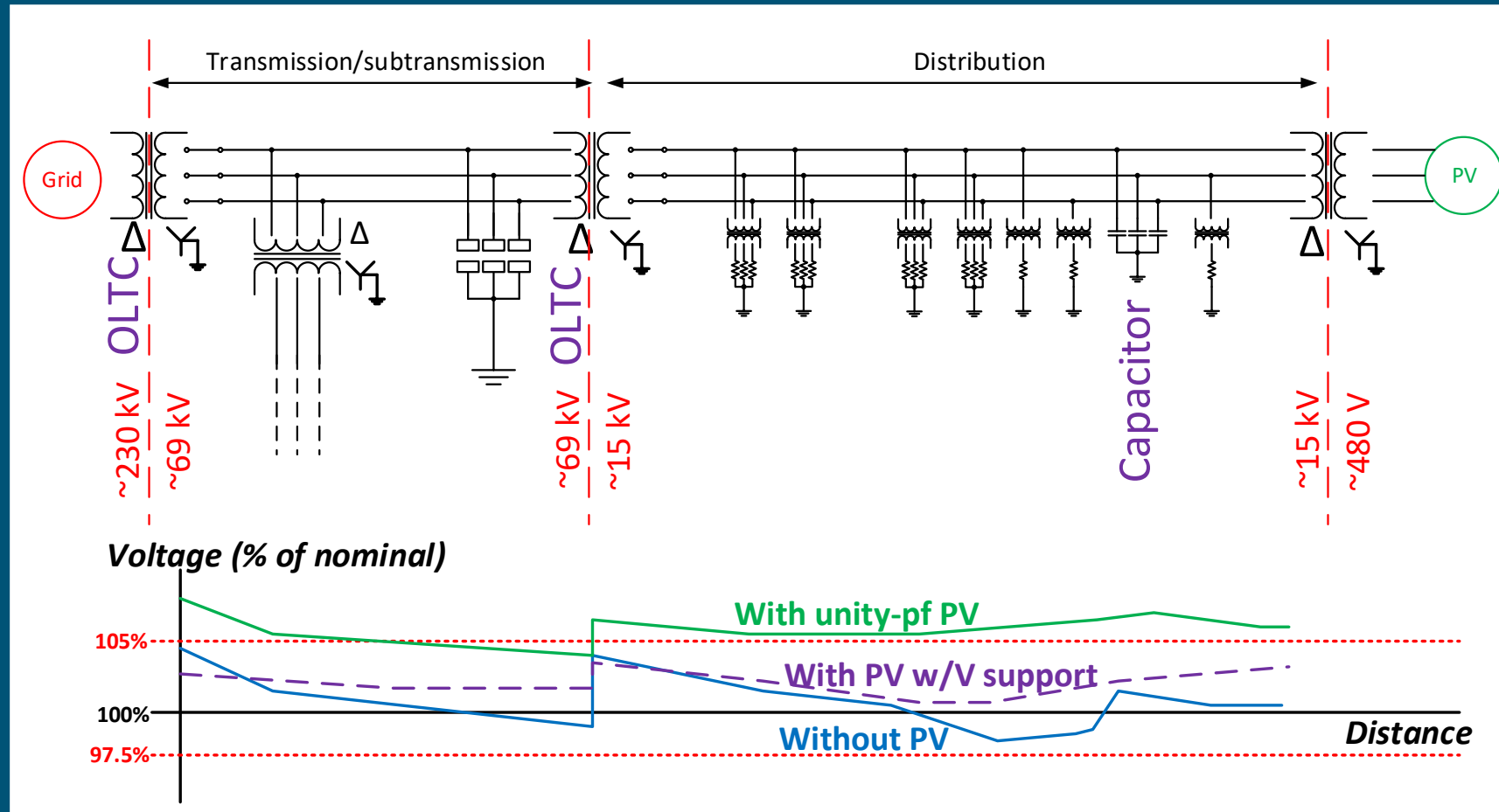


**IEEE Std 1547-2018<sup>TM</sup> and IEEE Std 1547-2020<sup>TM</sup> mandate that inverters provide tools to solve many of these challenges. Key examples:**

- ❑ Several inverter modes to help keep local voltages within tolerances
- ❑ Low voltage and low frequency ride-throughs (helps support the larger system when things go bad)
- ❑ Frequency support functions (also about supporting the larger system in bad times)
- ❑ Interoperability requirements (make sure devices can talk to each other and the utility—cybersecurity is addressed separately)



# Challenge #1: voltage regulation



Challenge: DER produces a “negative voltage drop”. Utility V regulators can’t control it.  
 Solutions: fixed-pf operation; volt-var and volt-watt controls; voltage regulation.

# Challenge #1: voltage regulation



IEEE Std 1547-2018™ provides new tools for dealing with this.

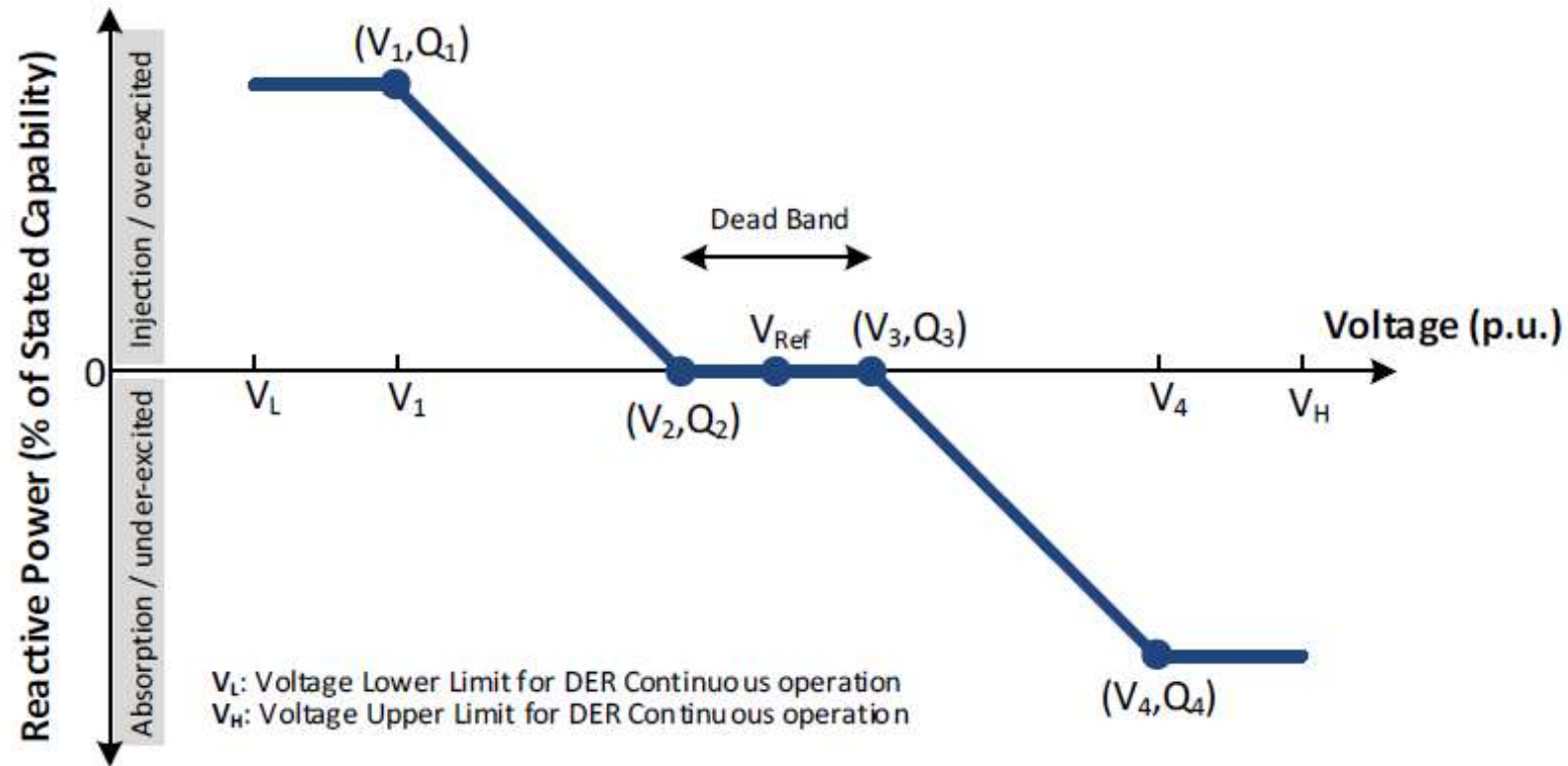


Figure H.4—Example voltage-reactive power characteristic

# Challenge #1: voltage regulation



## How well do these solutions work?

### Fixed-pf operation (most common solution)

- ✓ Simple; inherently stable (no interactions between inverters)
- ✗ Requires the utility to supply more vars; doesn't change if new PV is added

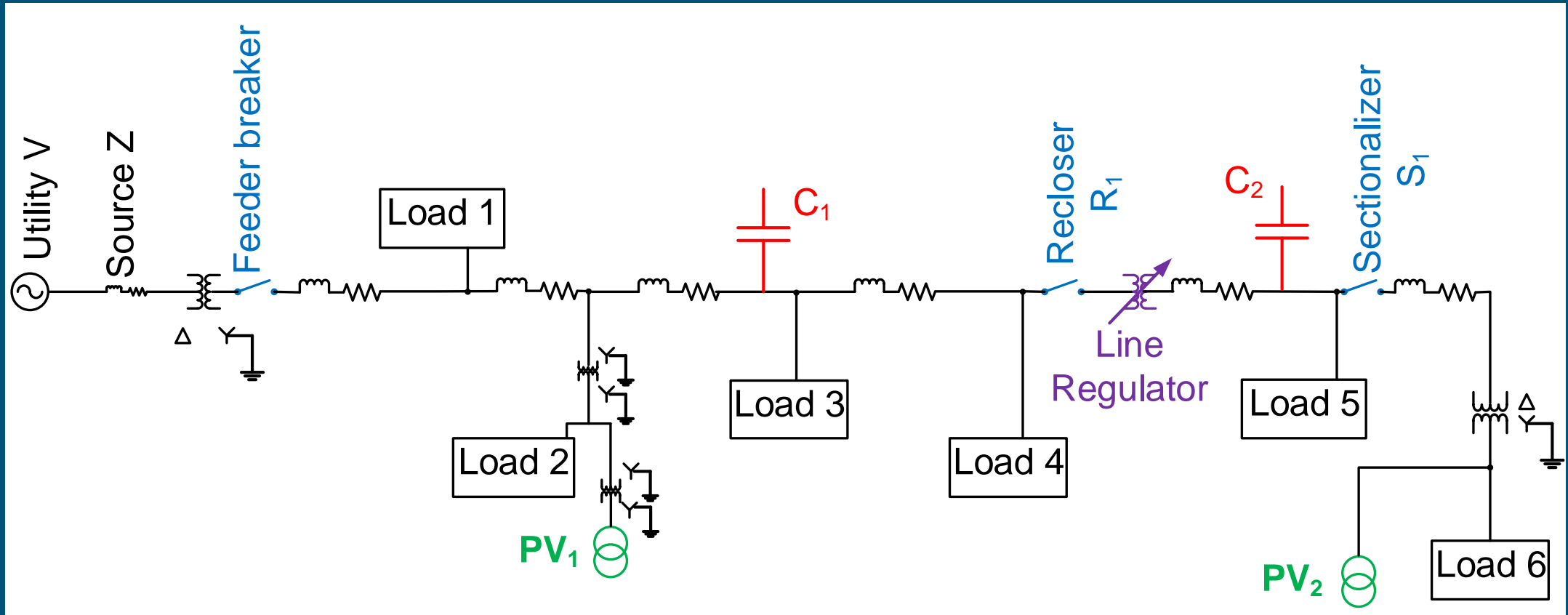
### Volt-var and volt-watt (usually implemented in plant controller @ PCC)

- ✓ Adaptively adjust output to help maintain healthy voltage
- ✗ Some possibility for inverters “fighting” with each other; usually requires PCC measurement; needs to be coordinated with CVR; can result in lower PV output

### Voltage regulation (implemented in plant controller @ PCC)

- ✓ Best voltage control; adapts to changing conditions; can significantly improve circuit voltage profile
- ✗ Must be set carefully to avoid inverters “fighting” with each other (may require comms); requires PCC measurement; has to be coordinated with CVR

## Challenge #2: unintentional islanding



Challenge: if generation balances load and a switch opens, DERs may not see it and continue to “run on”. **(VERY LOW-PROBABILITY EVENT.)**

Solution: today, inverter-resident active anti-islanding. Tomorrow: wide-area communications-based methods.

## Challenge #2: unintentional islanding



### How well do these solutions work?

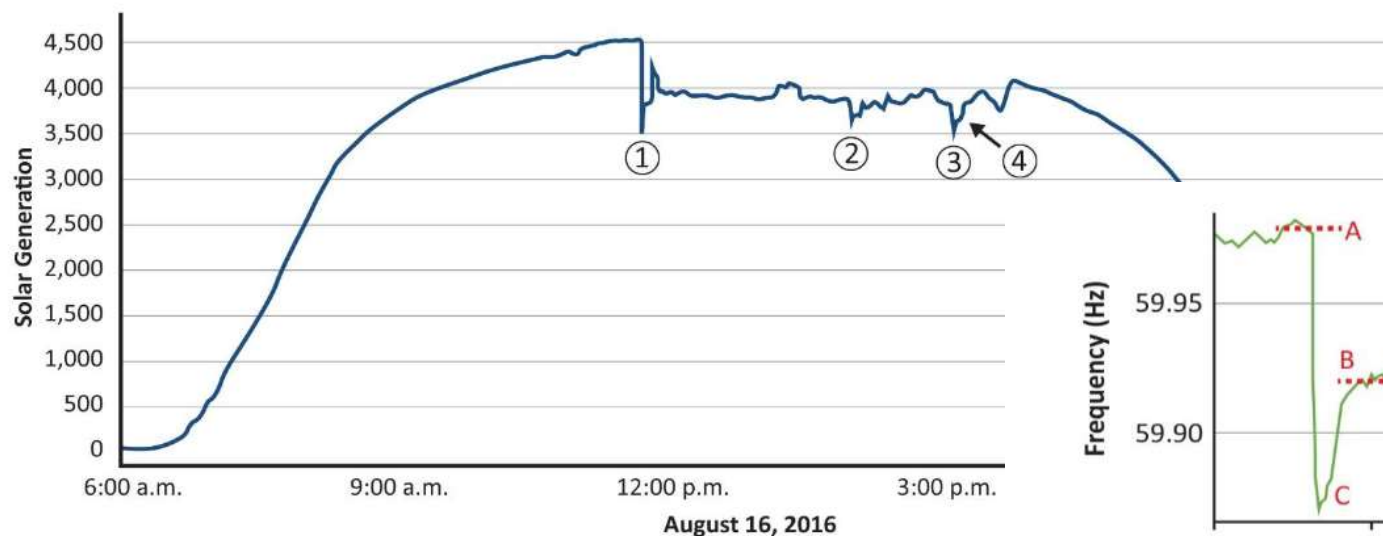
#### Inverter-resident active anti-islanding

- ✓ Extremely effective if all inverters are doing the same thing; still works well even with grid-support functions active
- ✗ Inverter-inverter interactions possible; can degrade system transient response if there are enough DERs

#### Wide-area communications-based methods

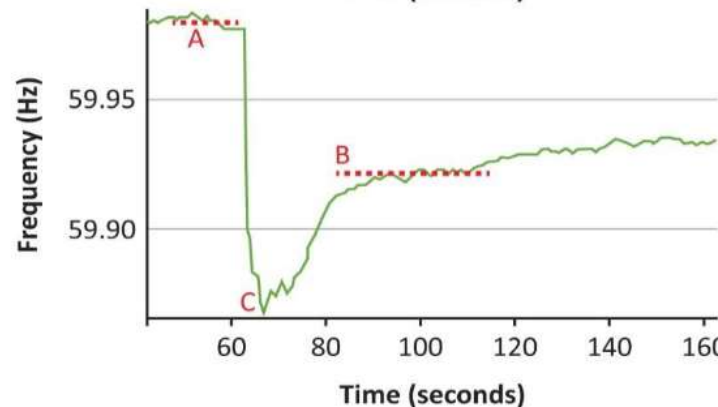
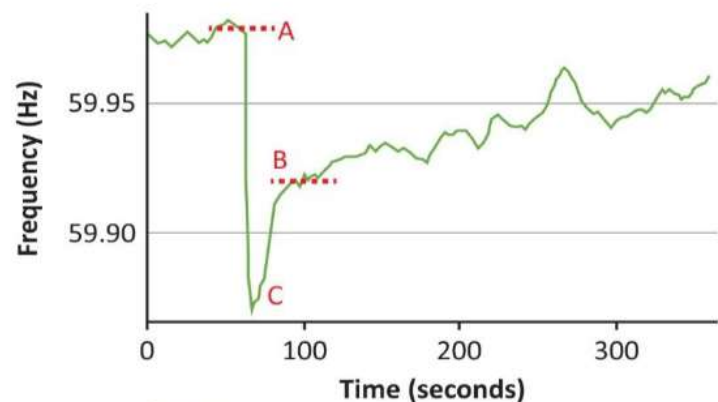
- ✓ Potentially an “ultimate” solution: DERs have system-level awareness they can use to detect unintentional islands, as well as provide intelligent grid support
- ✗ High cost is a barrier; also need further field demonstration of effectiveness

# Challenge #3: PV and bulk system dynamics



**Figure 1.3: Utility-Scale Solar PV Output in SCE Footprint on August 16, 2016**

Over 1000 MW of large PV tripped during a system event when it shouldn't have. There was a measurable, negative bulk-system impact.



Event ID: WI\_20160816\_184506  
 UTC Time: 08/16/2016 18:45:06  
 Local Time: 08/16/2016 11:45:06  
 Time Zone: PDT  
 M4 Flag: Yes  
 BAL003 Flag: Yes  
 MW Loss: 0  
 Value A: 59.979  
 Value B: 59.92  
 Point C: 59.8669  
 Time of C: 4.7  
 Point C': -  
 Time of C': -  
 A-B [mHz]: 59  
 A-C [mHz]: 112  
 FRM\_B [MW/0.1Hz]: 0  
 FRM\_C [MW/0.1Hz]: 0

**Figure 1.2: Western Interconnection Frequency during Fault**



What is being done to alleviate this?

IEEE Std 1547-2018™  
and IEEE Std 1547.1-2020™.

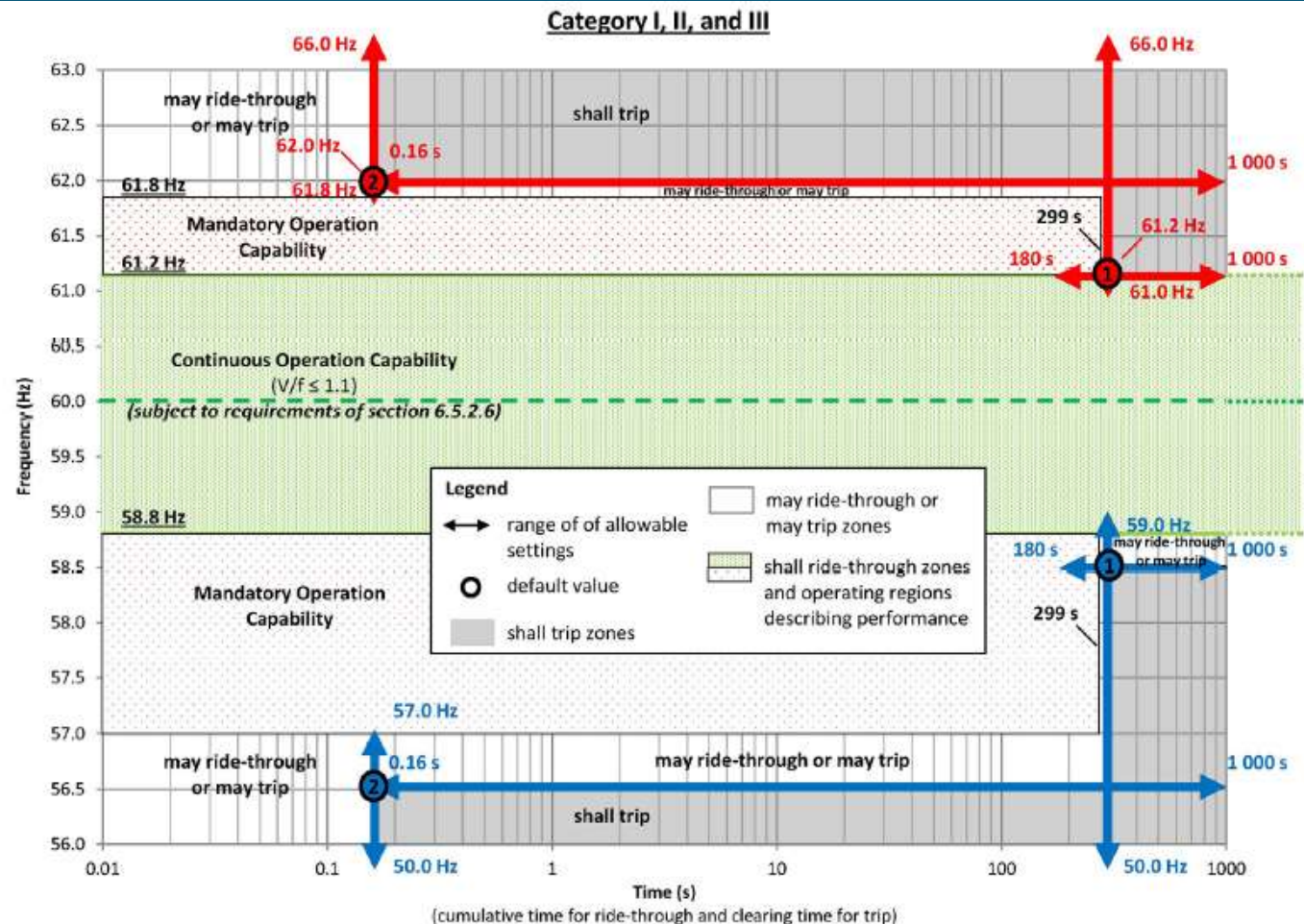
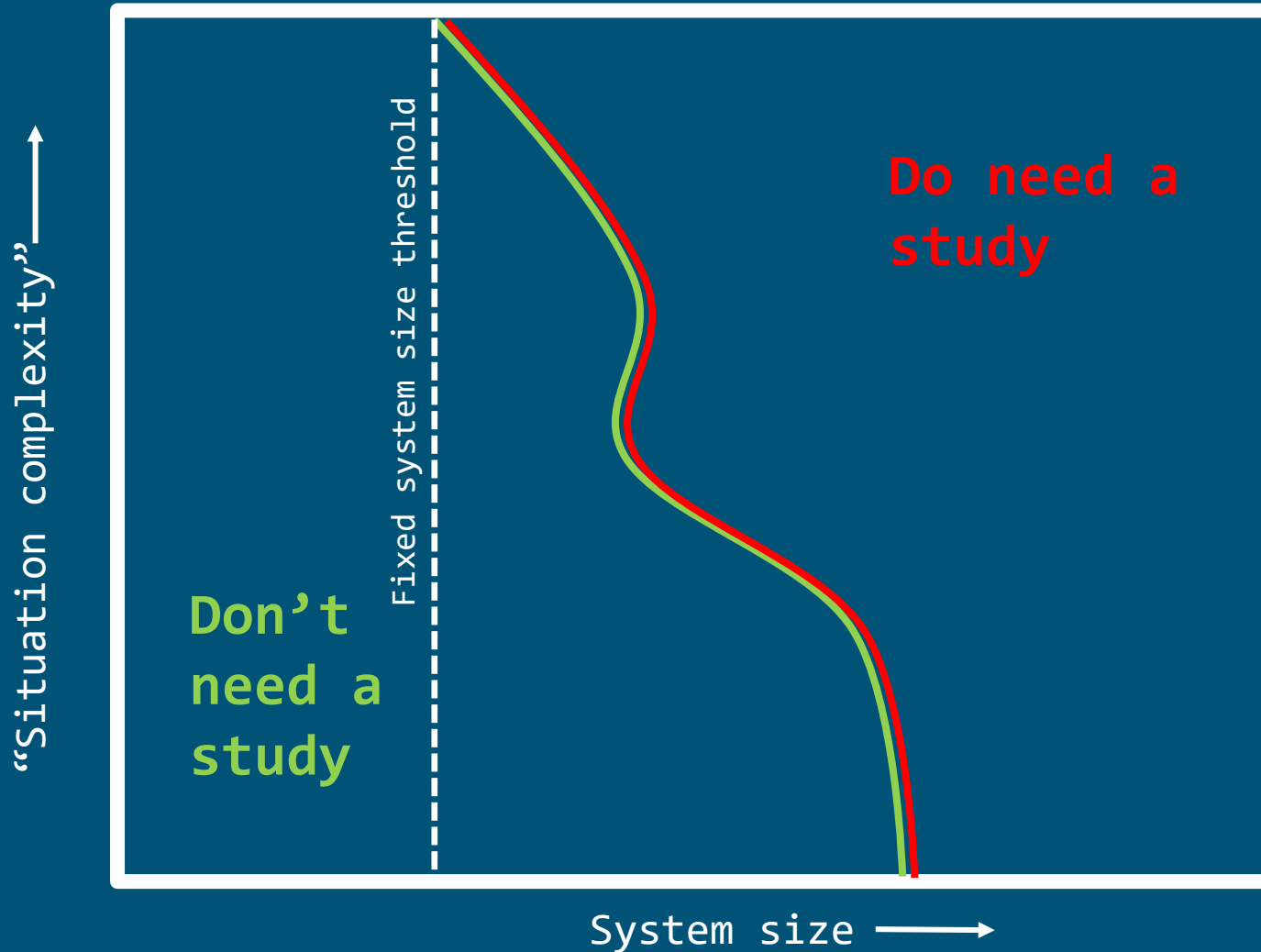


Figure H.10—DER default response to abnormal frequencies and frequency ride-through requirements for DER of abnormal operating performance Category I, Category II, and Category III



## DERs we want to interconnect

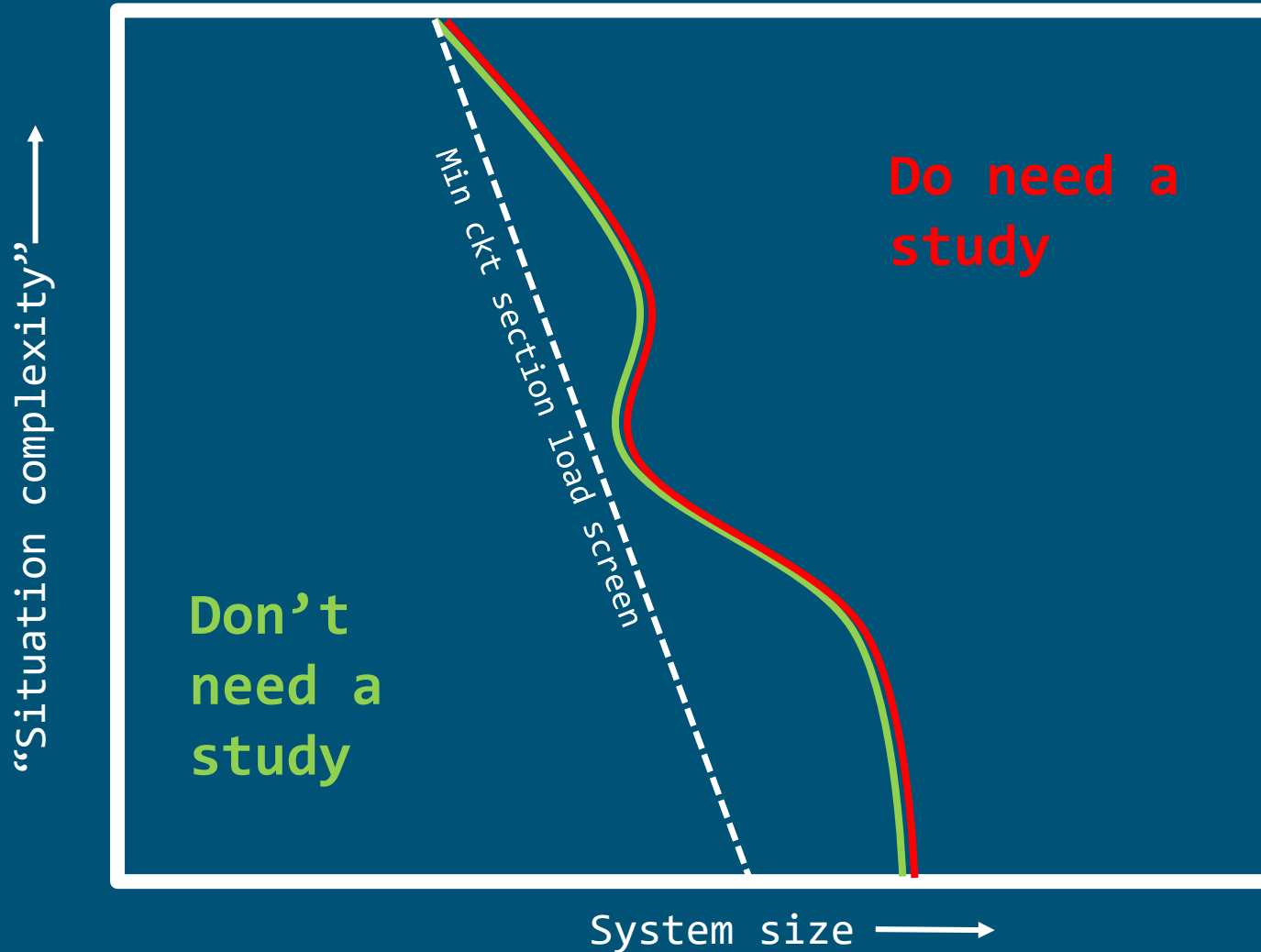


A fixed-system-size threshold is very simple, but also simplistic in the sense that a lot of unnecessary studies will be triggered.





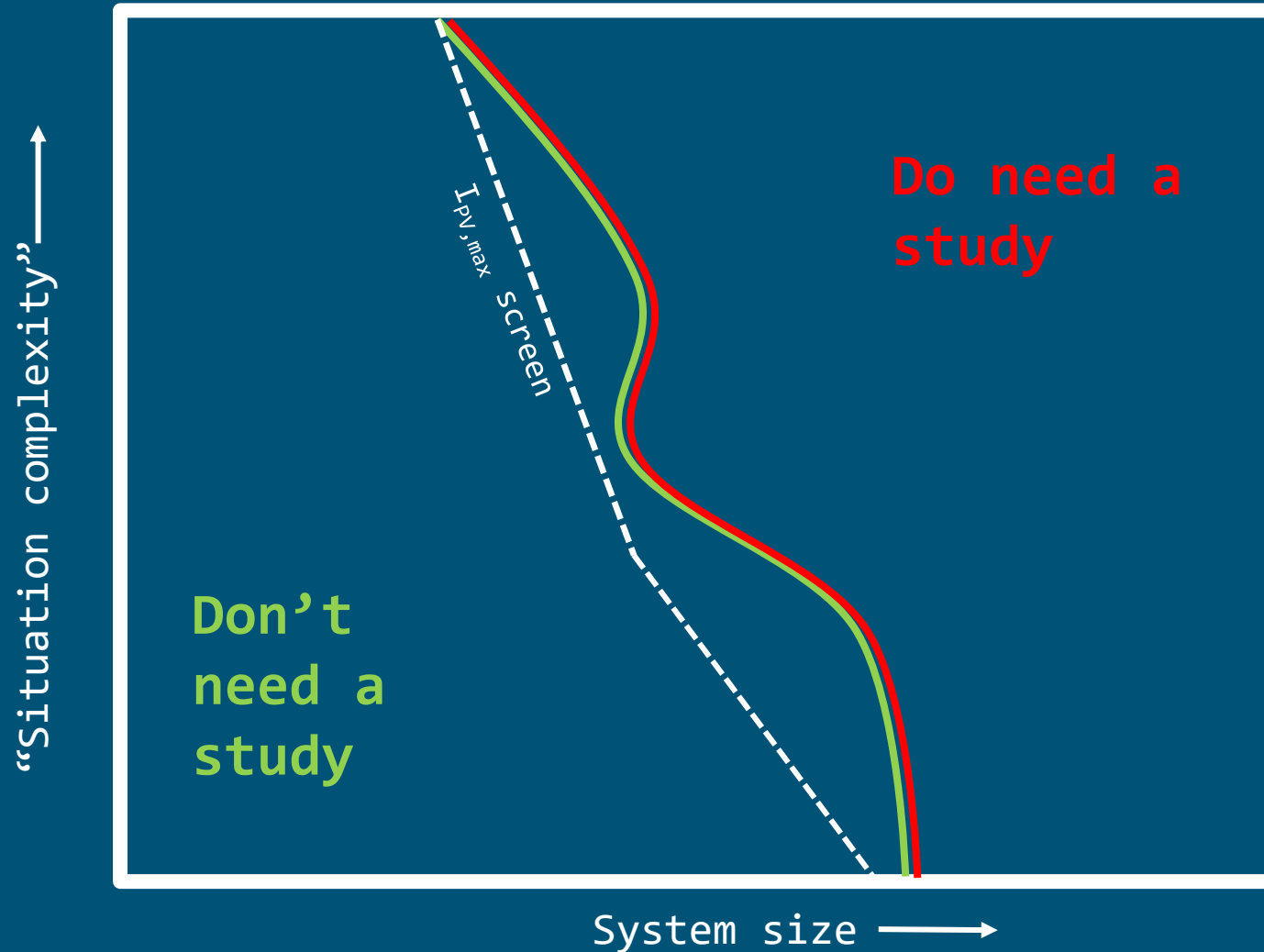
## DERs we want to interconnect



Going to a minimum circuit section load screen leads to a variable system size threshold, "trimming" the number of unnecessary studies.



## DERs we want to interconnect

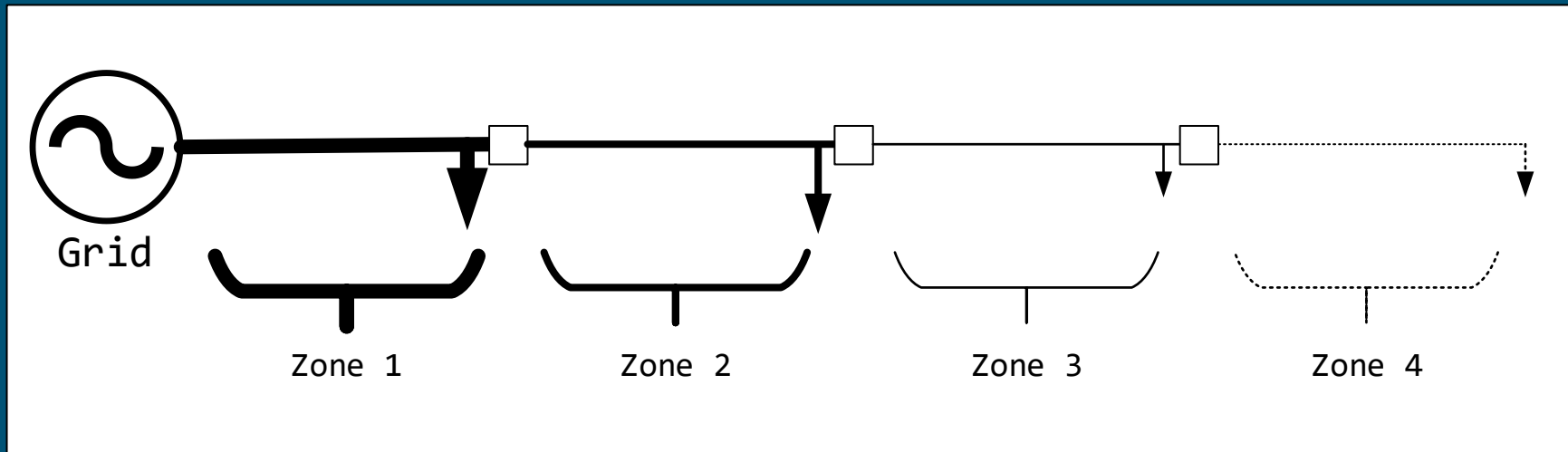


A more complex screen with more decision elements can cause the screen to match more closely with the boundary line.

## DER hosting capacity screens—how much IBR is OK?



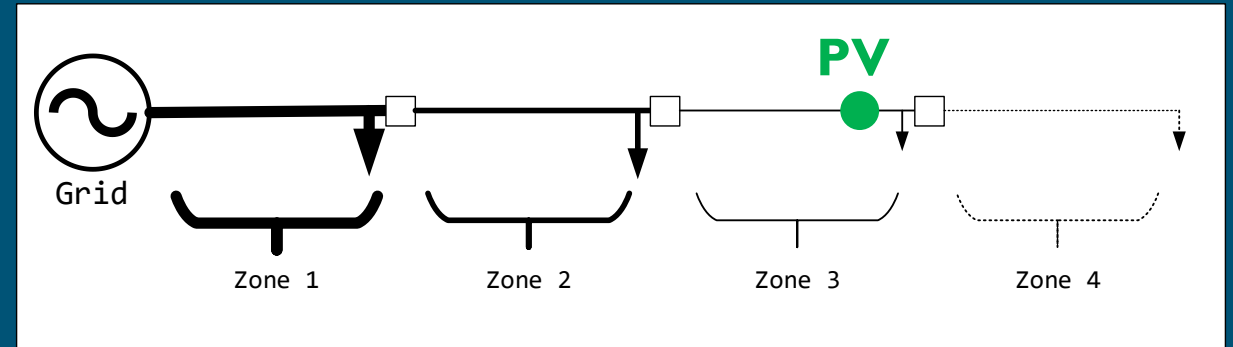
- Up to 100% of minimum load (minimum *daytime* load for PV), per circuit section/zone. At 100% of minimum zone load, DER is producing only as much current as that zone was already designed to handle. Addresses steady-state overvoltage, and thermal overload.



A possible alternative:

$$I_{PV,max} = \frac{V_{rise,max}}{Z_{source,max}}, \text{ subject to}$$

$$\|I_{PV,max}\| < I_{ampacity,min}$$



So if we're putting PV at the green dot,  $Z_{source,max}$  is the maximum source impedance from that point (including contingencies), and  $I_{ampacity,min}$  is the minimum cable ampacity in the path to the source (here, the ampacity in Zone 3).  $V_{rise,max}$  is typically 5% of the nominal voltage.

*This is very similar to what most utilities do when developing hosting capacity maps.*

Thank you!



Please feel free to email me with questions:

[meropp@sandia.gov](mailto:meropp@sandia.gov)

Special thanks to Dr. Imre Gyuk, DOE – Office of Electricity,  
Energy Storage Program.