PV Inverter Performance and Reliability: What is the Role of the Bus Capacitor?

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***Abstract*— In order to elucidate how the degradation of individual components affects the state of the photovoltaic inverter as a whole, we have carried out SPICE simulations to investigate the voltage and current ripple on the DC bus. The bus capacitor is generally considered to be among the least reliable components of the system, so we have simulated how the degradation of bus capacitors affects the ripple at the DC terminals of the PV module. Degradation-induced ripple leads to an increased degradation rate in a positive feedback cycle. By understanding the degradation mechanisms and their effects on the inverter as a system, steps can be made to more effectively replace marginal components with more reliable ones, increasing the lifetime and efficiency of the inverter and decreasing its cost per watt towards the US Department of Energy goals.**

***Index Terms*—BOS, Capacitor, Inverter, Photovoltaics, Power Electronics, Reliability**

I. Introduction

The Department of Energy (DOE) SunShot Initiative aims to decrease the costs of photovoltaic (PV) systems by 75% before the end of the decade, in order for PV systems to reach economic competitiveness with conventional energy sources. It is estimated that with an installed system cost of $1/Watt ($0.05-0.06/kWh) [1], PV penetration into the US power market will be upwards of 18% by 2050.

As of 2010, the installed cost of PV systems was $3.40/Watt [1]. While most research, both historically and currently, focuses on the production costs of PV module technology, the cost of the necessary grid-connected and/or stand-alone DC-to-AC inverters has been largely ignored. As the price of PV modules drops, the price of inverters becomes more important. Inverters and associated power conditioning components now constitute 8-12% of the total lifetime PV cost [2] at $0.25/Watt [3], well above the DOE 2017 benchmark of $0.10/Watt [1].

One of the key price drivers of inverter costs is reliability [4, 5]. PV modules now have long lifetimes with warranties offered up to 20 years and mean time between failures in the field of up to 522 years for residential and 6,666 years for utility systems [6]. In contrast, the inverter has shown a field mean time between failure of 1-16 years [7] with typical warranties lasting only 3-5 years [5] and occasionally (e. g. certain units by PV Powered) up to ten years.

In short, inverter technology must become half as costly and twice as reliable to facilitate grid-parity of solar energy in the future [5, 8]. Inverter reliability typically tends to be short because the inverter is both expected to serve a large number of functions (e.g. PV power management, grid connection/disconnection, VAR management, and/or island monitoring [2]) while operating in relatively harsh, changing conditions (-30-70˚C, 0-100% humidity, high salinity, etc). Many sources [2, 9] consider bus capacitors to be among the most unreliable elements of the inverter, decreasing the inverter lifetime as much as 50% [10] due to temperature and power cycling [11] resulting in high internal temperatures [12]. Capacitors represent the constituent that can most easily be altered in the short term to increase inverter lifetime and decrease lifetime PV system cost.

The purpose of an inverter is to transform a DC waveform voltage into an AC signal in order to inject power into a load (e.g. the power grid) at a given frequency and with a small phase angle ($\phi \approx 0$). A simplified circuit for a single phase unipolar Pulse-Width Modulation (PWM) is shown in Figure 1 (the same general scheme can be extended to a three phase system). In this schematic, a PV system, acting as a DC voltage source with some source inductance, is shaped into an AC signal through four IGBT switches in parallel with freewheeling diodes. These switches are controlled at the gate through a PWM signal, which is typically the output of an IC that compares a carrier wave (usually a sine wave of the desired output frequency) and a reference wave at a significantly higher frequency (typically a triangle wave at 5-20kHz). The output of the IGBTs is shaped into an AC signal suitable for use or grid injection through the application of various topologies of LC filters.

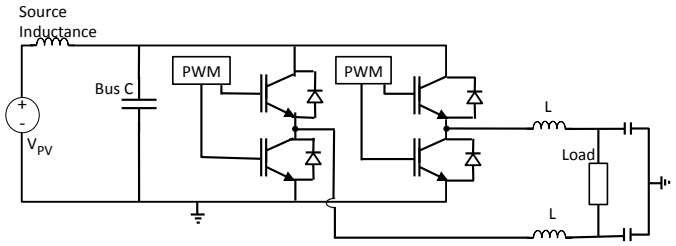

Figure 1: Pulsed Width Modulation (PWM) single-phase inverter setup. The IGBT switches, along with LC output filter, shape the DC input signal into a usable AC signal. This induces a

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deleterious voltage ripple across the PV terminals. The bus capacitor is sized in order to reduce this ripple.

The operation of the IGBTs introduces a ripple voltage onto the terminal of the PV array. This ripple is deleterious to the operation of the PV system, since the nominal voltage applied to the terminals should be held at the max power point (MPP) of the IV curve in order to extract the most power. A voltage ripple on the PV terminals will oscillate the power extracted from the system [13], resulting in a lower average power output (Figure 2). A capacitor is added onto the bus in order to smooth out the voltage ripple [14].

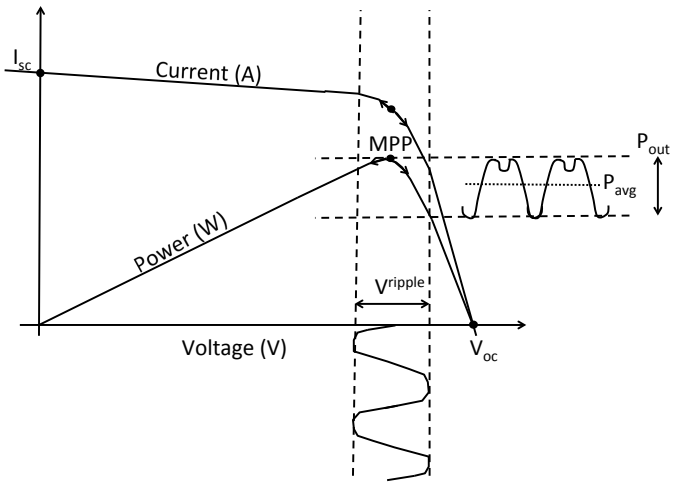

Figure 2: A voltage ripple introduced onto the PV terminals by the PWM inverter scheme shifts the applied voltage off the max power point (MPP) of the PV array. This introduces a ripple in the power output of the array so that the average output power is lower than the nominal MPP [13].

The amplitude (peak to peak) of the voltage ripple is determined by the switching frequency, PV voltage, bus capacitance, and filter inductance according to:

$$V_{p-p}^{ripple} = \frac{V_{PV}}{32 \cdot C_{bus} \cdot L \cdot f_{PWM}^2} \qquad (1)$$

where:
V_{PV} is the solar panel DC voltage,
C_{bus} is the capacitance of the bus capacitor,
L is the inductance of the filter inductors,
f_{PWM} is the switching frequency.

Equation (1) applies to an ideal capacitor that prevents charge from flowing through the capacitor during charging and then discharges the energy located in the electric field with no resistance. In reality, no capacitor is ideal (Figure 3) but is composed of multiple elements. In addition to the ideal capacitance, the dielectric is not perfectly resistive and a small leakage current flows from the anode to cathode along a finite shunt resistance (R_{sh}), bypassing the dielectric capacitance (C). When current through the capacitor is flowing, the pins, foils, and dielectric are not perfectly conducting and there is an equivalent series resistance (ESR) in series with the capacitance. Finally, the capacitor does store some energy in the magnetic field, so there is an equivalent series inductance (ESL) in series with the capacitance and ESR.

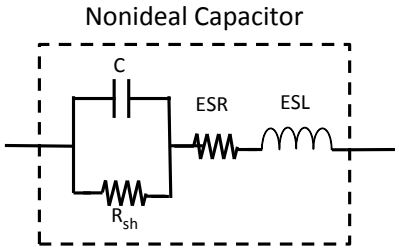

Figure 3: Equivalent circuit of a generic capacitor. A capacitor is composed of many non-ideal elements, including dielectric capacitance (C), a non-infinite shunt resistance through the dielectric that bypasses the capacitor, series resistance (ESR), and series inductance (ESL).

Even in a component as seemingly simple as a capacitor, there exist multiple elements that can fail or degrade. Each of these elements can affect the behavior of the inverter, both on the AC and DC sides. In order to determine the effect degradation of non-ideal capacitor components has on the voltage ripple introduced across the PV terminals, a PWM unipolar H-bridge inverter (Figure 1) was simulated using SPICE. The filter capacitors and inductors are held at 250μF and 20mH, respectively. The SPICE models for the IGBTs are derived from the work of Petrie et al. [15]. The PWM signal, which controls the IGBT switches, is determined by a comparator and inverting comparator circuit for the high- and low-side IGBT switches, respectively. The input for the PWM controls are a 9.5V, 60Hz sine carrier wave and a 10V, 10kHz triangular wave.

II. Simulation Results and Discussion

Figure 4 shows the results of a SPICE simulation for a 250μF bus capacitor. The output of the inverter across the load is an AC wave at 60Hz. The bus voltage, though nominally 310VDC, contains an AC ripple with a frequency of 120Hz. The inset of Figure 4 shows a close-up of the bus voltage and demonstrates that, in addition to the 120Hz ripple, there exists a high frequency component to the ripple. This high frequency is equal to the PWM triangle wave frequency.

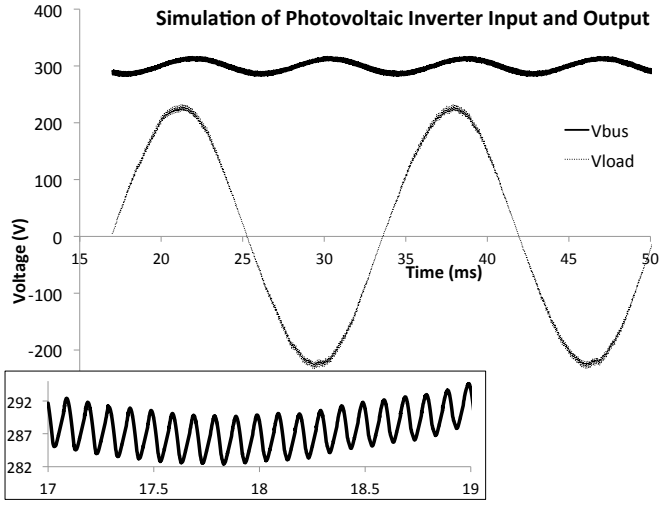

Figure 4: Results of SPICE simulation of inverter circuit. The IGBT switching transforms the nominal DC bus voltage from the PV array into an AC signal across the load. This induces a ripple at 120Hz. The inset shows an expanded view of the bus voltage, showing a ripple at the PWM frequency.

Correctly sizing the bus capacitance according to (1) is typically used to manage this DC-side ripple voltage. Simulations correctly predict the voltage ripple on the bus as a function of the bus capacitance (Figure 5). The ripple has a 1/C dependence, as predicted. For a 325V bus voltage, the ripple dramatically increases as the capacitance decreases, with relatively little decrease for capacitances above ~370μF.

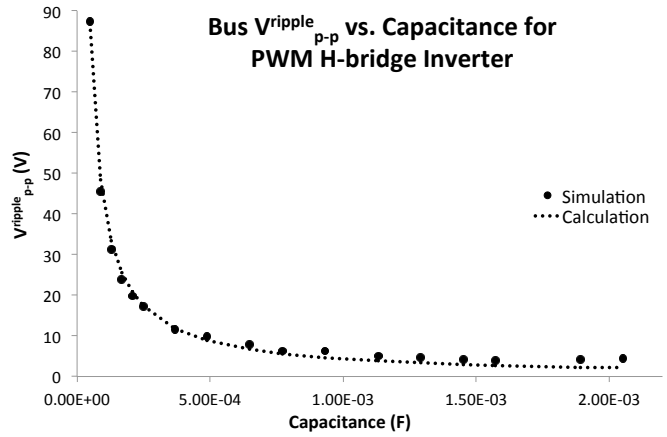

Figure 5: SPICE simulations of bus ripple correctly match the expected results from (1).

Although correctly sizing the bus capacitance is important to control the magnitude of the bus ripple, it is not the only thing that must be considered. The component frequencies of the bus ripple, which are influenced by the source inductance, are quite important. Both the size of the bus capacitor and source inductance will affect the resultant DC-side ripple. Those components will interact to form an LC oscillator circuit, which will cause the inverter circuit to resonate (ring) at a frequency determined by (2). This can be very detrimental to the system if the frequency of ringing corresponds either to the PWM frequency or a multiple of the carrier wave frequency.

$$f_{ring} = \frac{1}{2\pi\sqrt{L_{source}C_{bus}}} \quad (2)$$

where:
f_{ring} is the ringing frequency,
L_{source} is the source inductance

Figure 6 shows the magnitude of the ripple voltage for an inverter system with a 250μF bus capacitor as a function of the source inductance. When the source inductance combines with the capacitance such that f_{ring} is equal to either the PWM frequency or a multiple of the carrier wave frequency according to (2), the magnitude of the ripple increases dramatically.

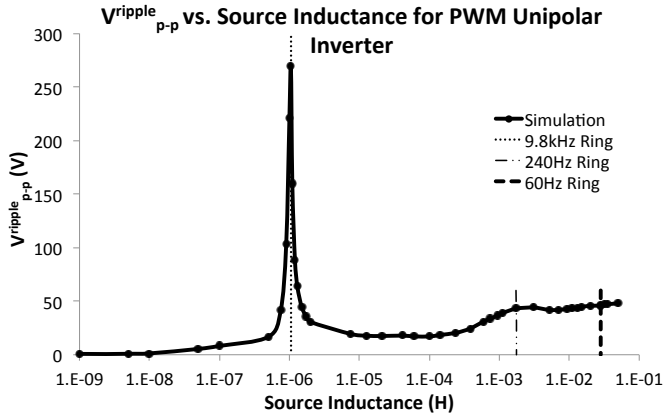

Figure 6: Ripple voltage for a PWM unipolar inverter with a 250μF bus capacitor as a function of the source inductance. The bus capacitor and source form an LC oscillating circuit that will ring at the PWM signal and multiples of the carrier wave frequencies.

As the inverter operates, the ripple on the DC bus will increase over time as the bus capacitor degrades. The exact behavior of the ripple depends on exactly which of the capacitor components degrade.

A large enough ESL will dramatically affect the bus ripple magnitude and frequency. However, the ESL of a typical commercial capacitor is quite small (~nH [16]) and is largely ignored in circuit analysis of capacitors. Since the ESL is typically small enough to go unnoticed and does not change much over the lifetime of the capacitor, it has not been investigated in this work.

The shunt resistance directly controls (and is inversely proportional to) the leakage current of the capacitor.

$$\frac{ESR}{ESR_o} = \frac{1}{1 - k \cdot t \cdot e^{\frac{-E_a}{T}}} \quad (3)$$

where:
ESR_o is the original ESR,
k is a constant dependent on the capacitor design, but is usually ~1.77 [20, 21]
t is time
E_a is an activation energy (≈4700 eV [22])
T is temperature (Kelvin)

Historically, electrolytic capacitors have suffered from increasing leakage currents over time due to corrosion effects [17]. However, state-of-the-art capacitors suffer almost no change in leakage current, even over long periods of time (for electrolytic capacitors, there is a short term decrease in leakage current due to oxide reformation effects). Shunt resistance effects on both the inverter input and output were investigated; however, the waveforms of both the AC and DC sides were found to be relatively unaffected by changes in shunt resistance until leakage current increased by a factor of ~100. As leakage current increases by 100-times above nominal levels, the inverter efficiency decreases exponentially (data not shown).

One of the primary degradation modes of capacitors is an increase in the ESR. Figure 7 shows the effect of ESR on DC-side voltage ripple. Voltage ripple magnitude is highly dependent on the size of the ESR before leveling off at high ESR values (>4Ω).

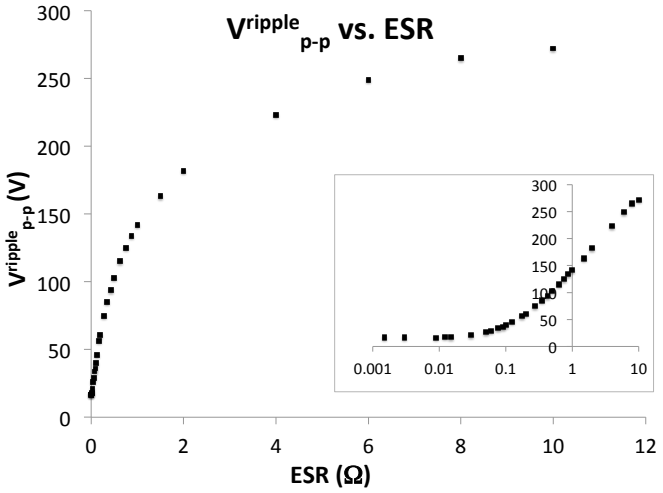

Figure 7: Inverter DC Ripple voltage vs. ESR for a bus capacitor. The DC ripple voltage magnitude is highly dependent on the size of the capacitor ESR. The inset shows the same graph on a semi-log plot to give greater detail regarding small ESR values.

Electrolytic capacitors have relatively high initial ESR values (~20mΩ, but up to 80mΩ for high voltage capacitors) compared to metallized thin film (~1mΩ) [14]. Additionally, the ESR of electrolytic capacitors tends to increase over the lifetime of a capacitor due to the consumption of H_2O during oxide reformation [18] or electrolyte evaporation [19]. Over time, the ESR of an electrolytic capacitor has been found to follow the linear inverse relationship first defined by Rhoads and Smith:

This equation gives an estimate of the best-case capacitor lifetime due only to electrolyte evaporation. Electrolyte evaporation is highly dependent on the operating temperature of the capacitor and the general "rule of thumb" for electrolytic capacitors is that a 10˚C increase in temperature decreases lifetime by a factor of two. Sandia National Labs has monitored the temperature of inverter components *in situ.* Bus capacitors can easily reach peak temperatures of ~60˚C, even for fairly modest ambient temperatures (~20˚C) in the late winter.

Figure 8 shows the magnitude of the DC ripple voltage as a function of the capacitor operating time according to (3) for a typical electrolytic bus capacitor that has an original ESR of 50mΩ and operates at an average temperature of 70˚C. Soft failure, defined as an ESR increase of 200%, is denoted by the hatched line and occurs after 71,000 hours of operation when the ripple voltage has reached a value of 40V.

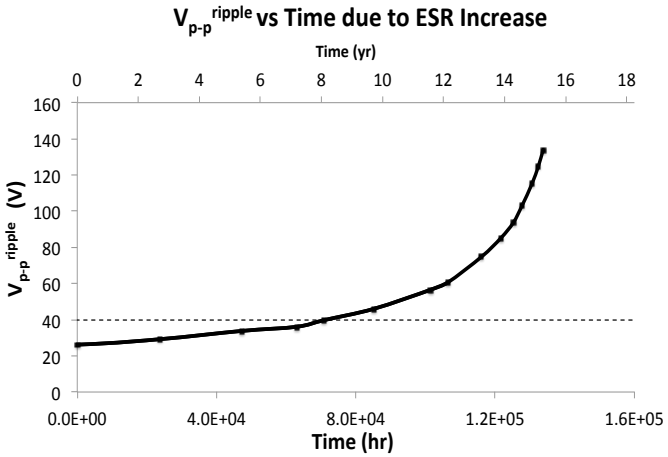

Figure 8: Ripple voltage vs. time for an electrolytic capacitor due to ESR increase according to (3). The dashed horizontal line indicates an increase in the ESR of 200%, a common definition for soft failure. In this typical bus capacitor, soft failure would be expected, in the best case, to occur after 71,000 operating hours with a ripple voltage of approximately 40V.

The expected lifetime of capacitors using this model is quite good (~70,000 hours), especially since failure is through slow degradation rather than a catastrophic event, so the capacitor continues to function, albeit in a reduced capacity. However, this is an ideal model for capacitor lifetime and does not take into account any effects of ripple current, which may significantly alter the interior temperature of the capacitor compared to the outer surface. This leads to a positive feedback mechanism between ESR and ripple current. In this cycle, as the ESR increases, the ripple voltage and current also increase. This increase in ripple current causes an increase in the capacitor core temperature, which causes further and faster degradation of the capacitor ESR.

This model also does not take into account how electrolyte evaporation affects capacitor integrity as the buildup of pressure inside the capacitor container may lead to

venting and leakage of liquid electrolyte long before the capacitor fails in a degradation mode. Finally, the model does not consider any decreased lifetime due to voltage acceleration. A capacitor would only be expected to have a 71,000 lifetime if it is sized (for ripple current, voltage, and temperature) well above actual working conditions, so that it would be relatively unstressed throughout its working life.

In a real world inverter, it is unlikely that a capacitor will only be subject to ideal conditions well below the capacitor sizing parameters. Often, the capacitor stress is increased for the sake of other components. For example, as the temperature of an inverter increases above a certain set point, the control circuitry of the inverter will de-rate the inverter output in order to decrease the internal temperature. For certain inverters, this is accomplished by increasing the voltage applied to the PV array towards the open circuit voltage. While this will successfully reduce the temperature by exponentially decreasing the current input to the inverter, it increases the voltage stress of the capacitor. So, for a de-rated inverter, the capacitor is doubly degraded, both from the increased temperature in the inverter and the increased bus voltage. This inverter behavior can be disastrous as the capacitor is only rated to a voltage at or slightly above the array open circuit voltage. Such a capacitor would not be expected to last through 71,000 operating hours.

Unfortunately, to reduce costs, some inverter manufacturers decide to sacrifice capacitor quality and/or size. Incorrect sizing of the capacitor or sizing without a complete understanding of the consequences to DC-side ripple can be disastrous and lead to shortened capacitor lifetimes. Short lifetimes are costly, not only due to replacement parts, but also due to system downtime, cost of replacement energy, and any reduced efficiency before failure identification.

III. Summary and Future Work

This work has investigated capacitor degradation effects on inverter operation, namely with regard to the voltage ripple onto the nominal DC supply voltage of the PV array. This ripple is deleterious, since it decreases average PV power output. SPICE simulations have been used to simulate the input and output of a PWM unipolar PV inverter utilizing IGBT switches. These simulations have shown that voltage ripple on the DC-side is composed of two distinct frequency components. There is a ripple at twice the carrier wave frequency and a ripple at the PWM frequency.

The magnitude of the DC ripple voltage has been shown to be affected both by the capacitor size and source inductance. The combination of these components forms an LC oscillator that, if the resonant frequency occurs at one of the ripple voltage component frequencies, can drastically increase the magnitude of the ripple voltage. Leakage current does not impact the inverter input or output for changes up to two orders of magnitude from nominal values. However, ripple voltage was found to be highly dependent on capacitor ESR. For electrolytic capacitors, this ripple voltage as a function of ESR can be transformed to a function of time through a linear inverse formula. Using this formula, it is estimated that an average inverter would be expected to operate for 71,000 hours before failure, at which point the ripple voltage would be 40V. However, this best-case formula does not take into account voltage stress or ripple current, so lifetimes of real world capacitors are expected to be much lower.

Sandia National Labs is currently conducting experiments on bus capacitor reliability. These efforts focus on metallized thin film capacitors for three reasons. First, there is a trend towards replacing electrolytic capacitors with metallized thin film capacitors, even for smaller residential systems. This push is driven both by the widely held view that thin film capacitors are inherently safer than electrolytics and that the increased cost of the thin film capacitors is compensated by their tolerance of higher ripple currents.

Second, most reliability data on metallized thin film capacitors are for pulsed power applications. While these experiments show excellent lifetimes (up to 150,000 hours [23]), some experiments have shown much shorter (<10,000 hours) lifetimes under constant voltage conditions [24-28].

Finally, thin film capacitors are said to be inherently safe compared to electrolytics due to self-clearing properties that prevent short-circuiting. Therefore, thin film capacitors should not fail catastrophically. However, since the number of clearing events increases exponentially after soft failure, the pressure inside the capacitor increases and may eventually lead to flashover and catastrophic failure. Future experiments will examine the failure behavior of thin film capacitors if they are used beyond their soft failure points to determine if they are significantly safer compared to electrolytic capacitors.

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