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"Development of the Medium Voltage PEBBs Using Gen3 10 kV SiC MOSFET Modules"

Medium Voltage PCB-based Bus Design and Insulation Coordination for Power Electronics Building Blocks

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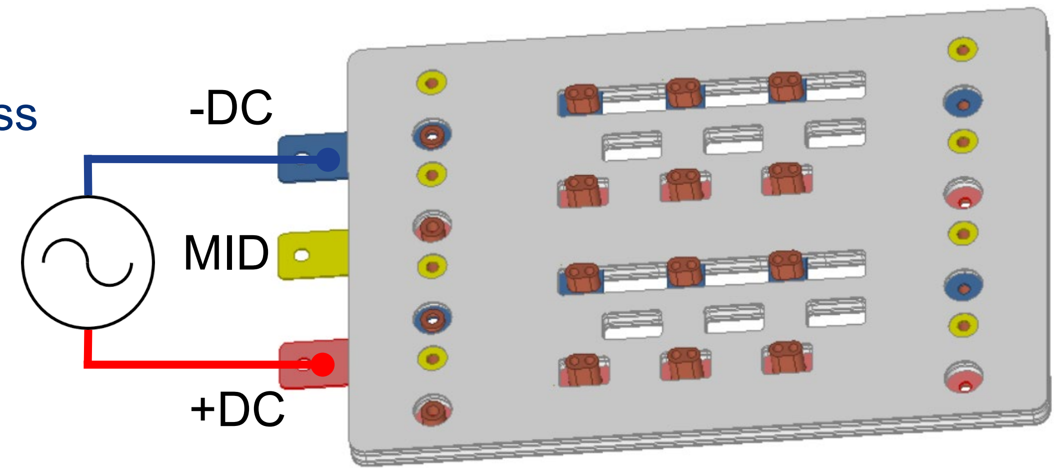
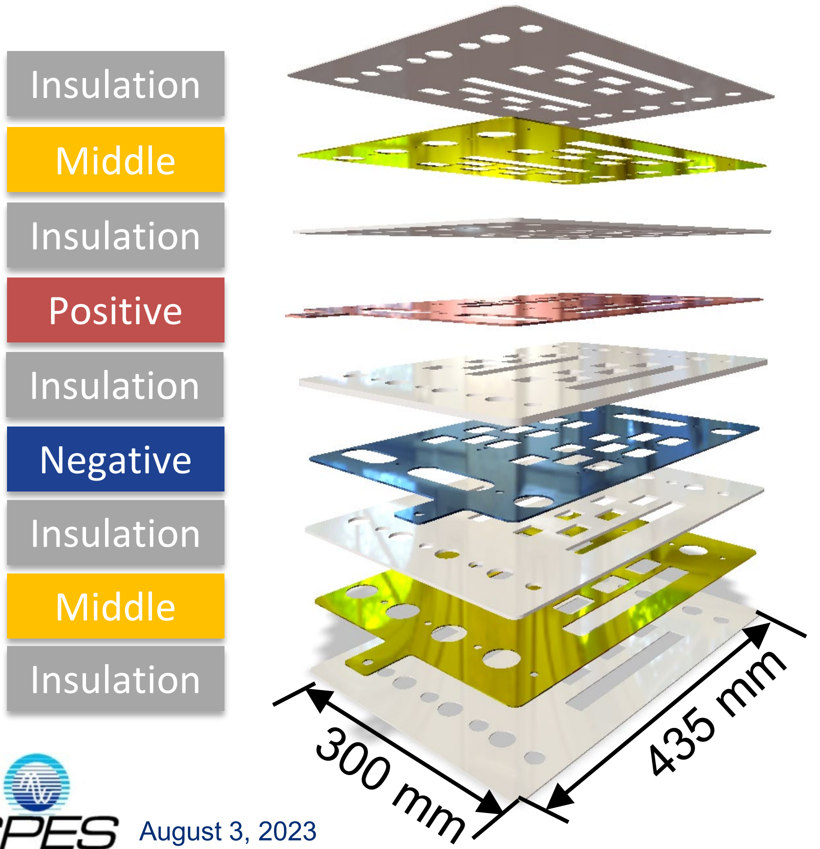
Outline

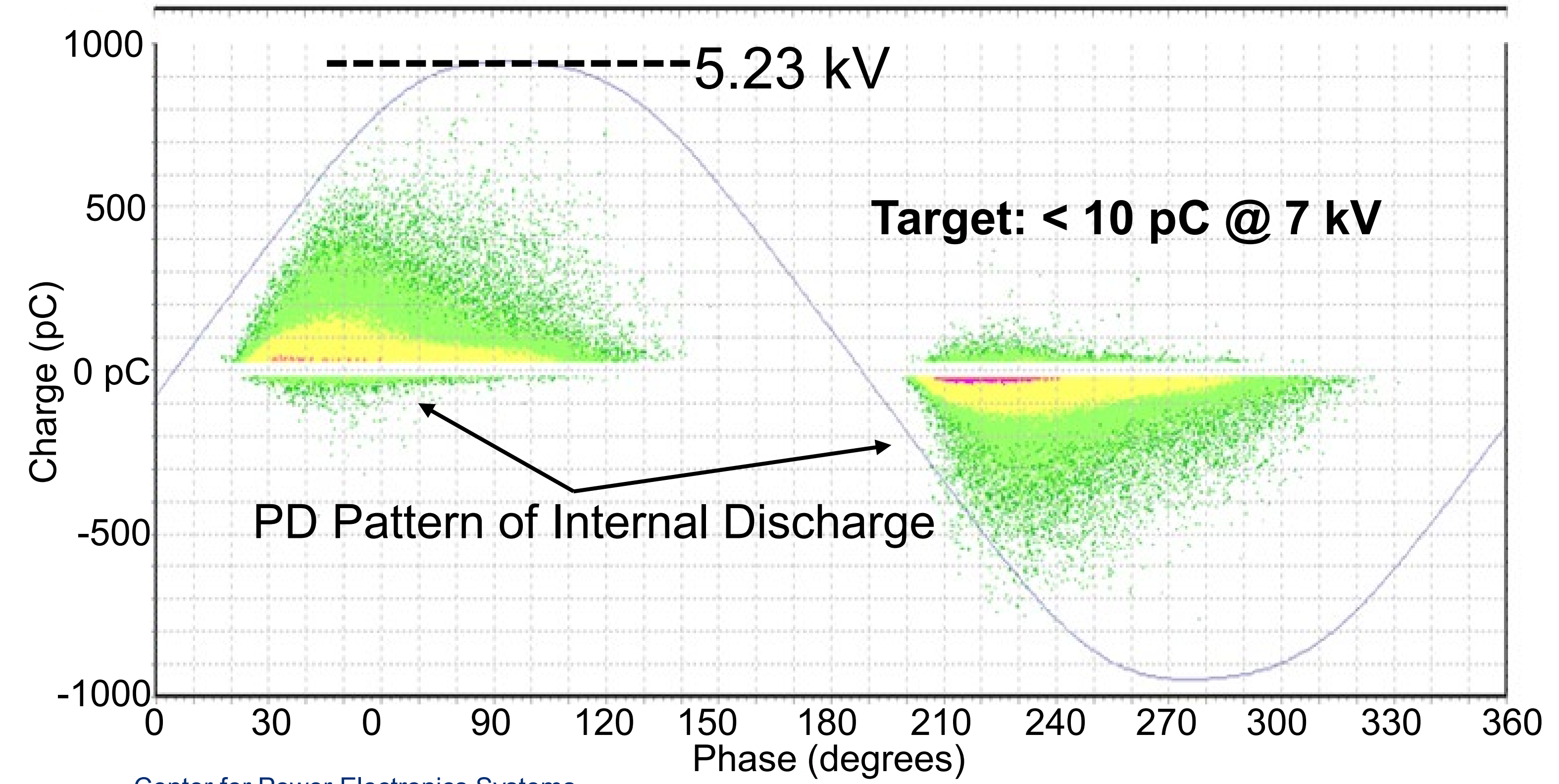
- Background
- Design Method for Medium Voltage PCB-based Components
- Medium Voltage Cooling System Design
- Summary & Conclusions

Insulation Challenges with Conventional Laminated Bus

- Low PDIV on conventional laminated bus; PDIV = 5.23 kV
  - Leading manufacturers recommended increasing thickness from 19 mm to 30 mm to reach target PDIV
- Heavy due to thick insulation and decoupling capacitors
  - 17.62 lb without decoupling capacitors
  - 25.8 lb with decoupling capacitors

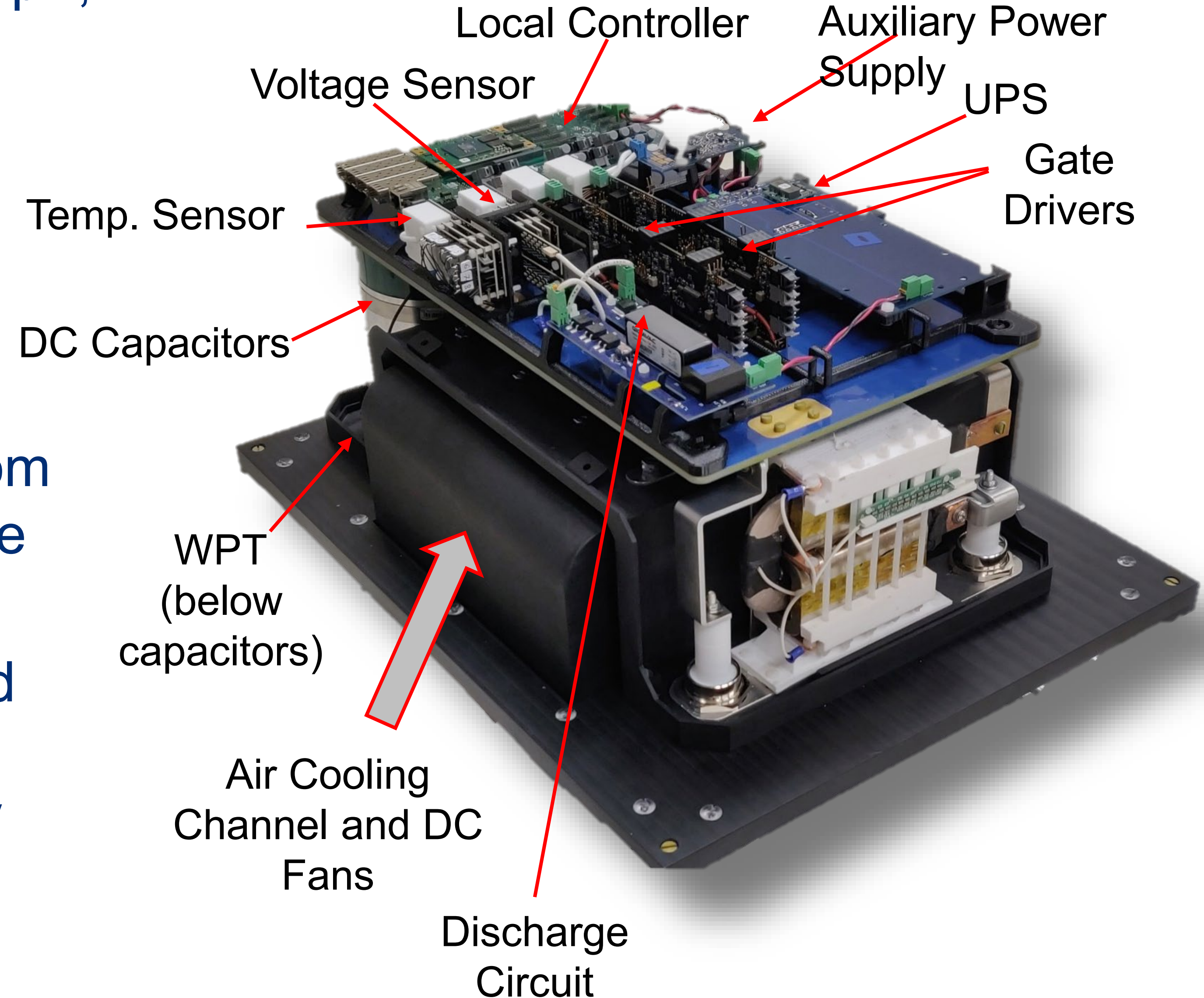






Insulation Design Challenges

- Medium voltage capacitors 3.5 kV, 60 µF, limit power density
- Maximum differential voltage within PEBB is 6 kV
  - ±3 kV maximum voltage across ancillary circuitry within PEBB
  - 30 kV maximum voltage to ground
- Auxiliary circuits can be located far from power supplies leading to long HV wire interconnection
- Fan array is fed from a 24-V-to-ground network
  - **Maximum voltage to heatsink is 27 kV**



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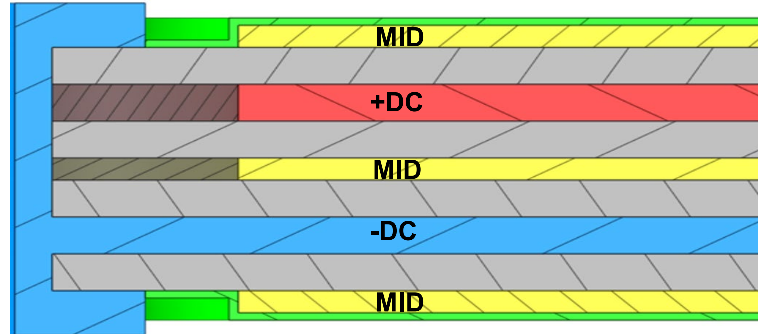
Method for Electric Field Evaluation

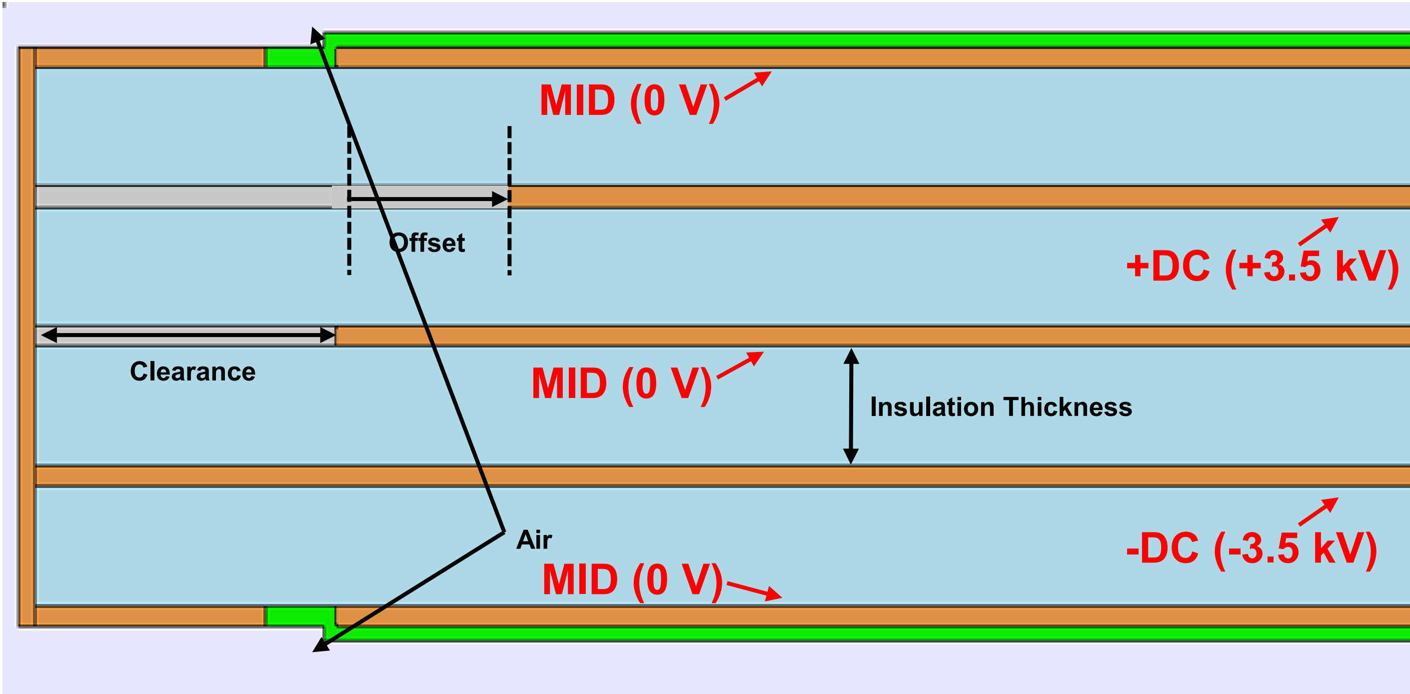
Design Goal

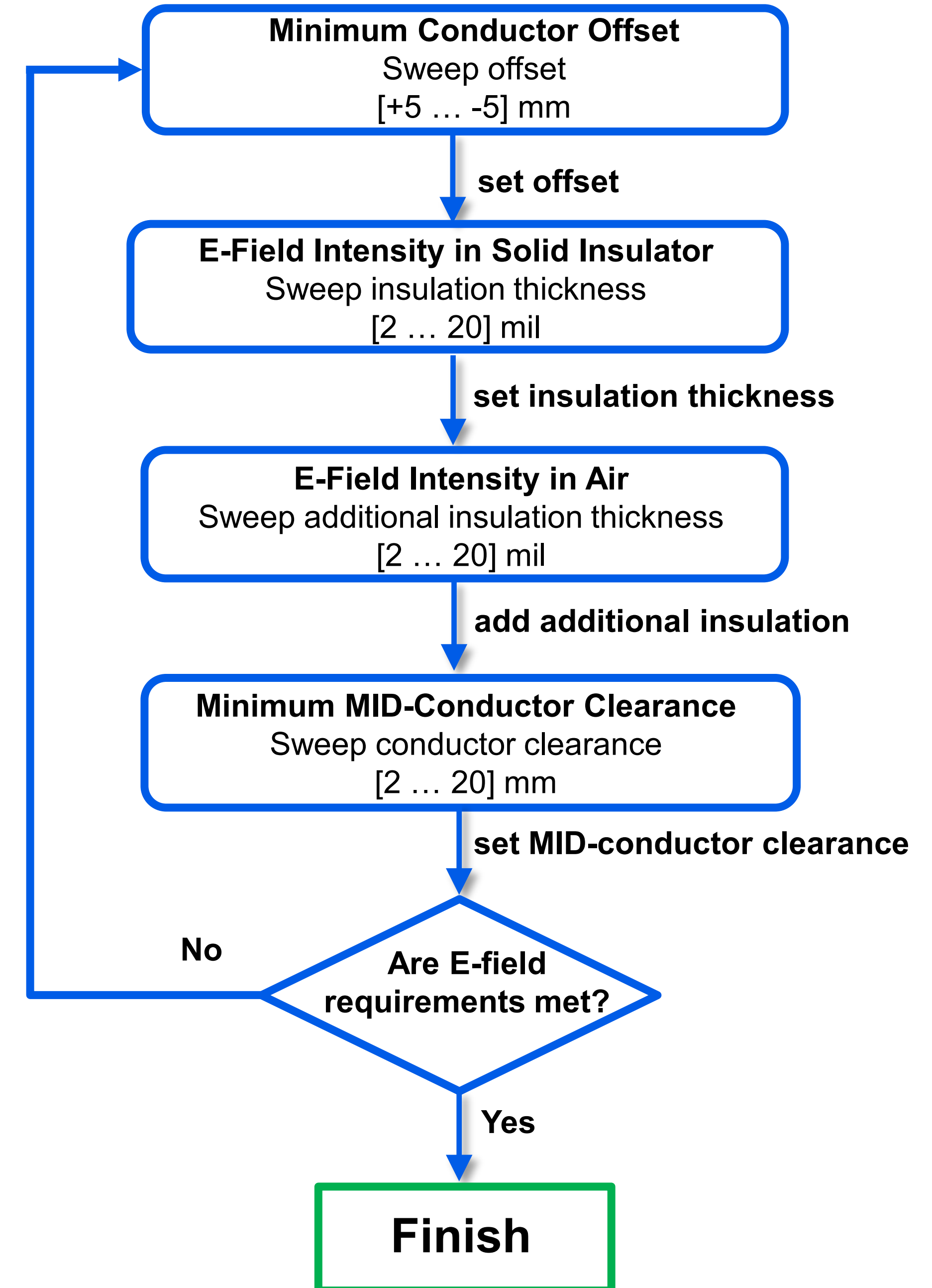
E-field control

1) Inside dielectric of PCB

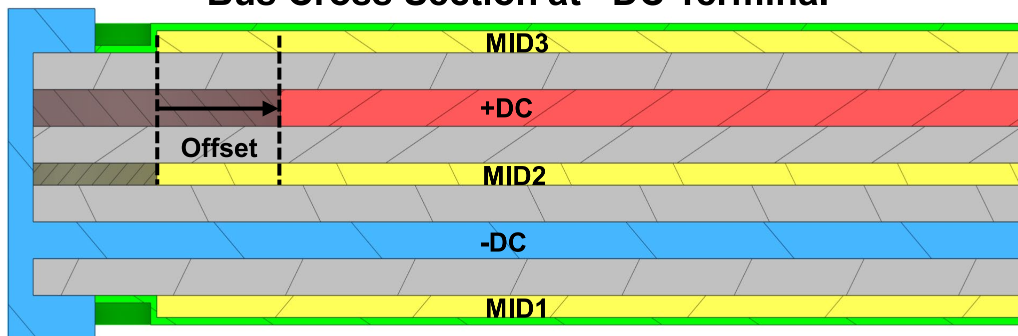
2) Along surface of PCB

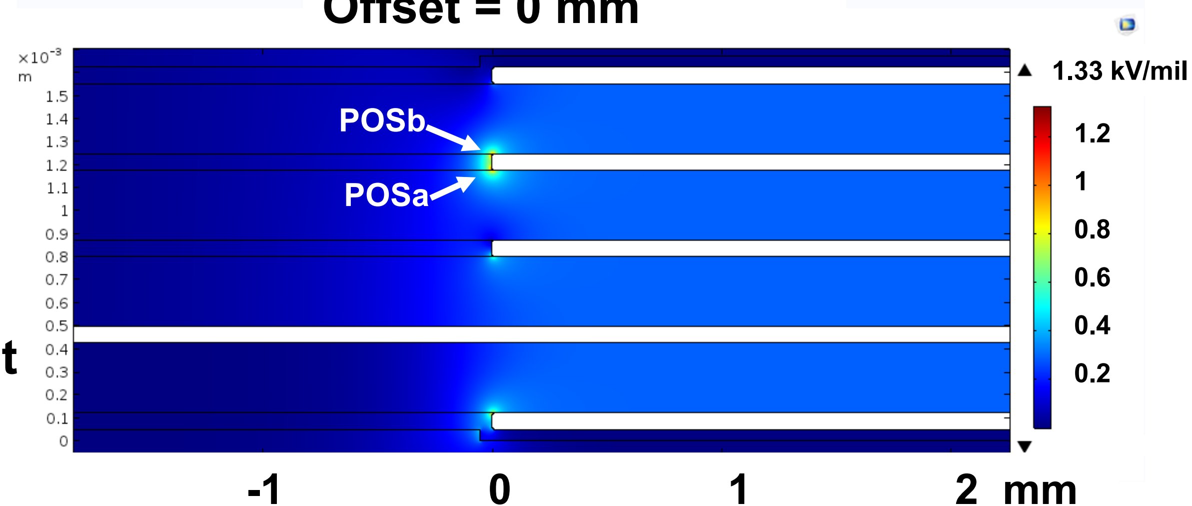


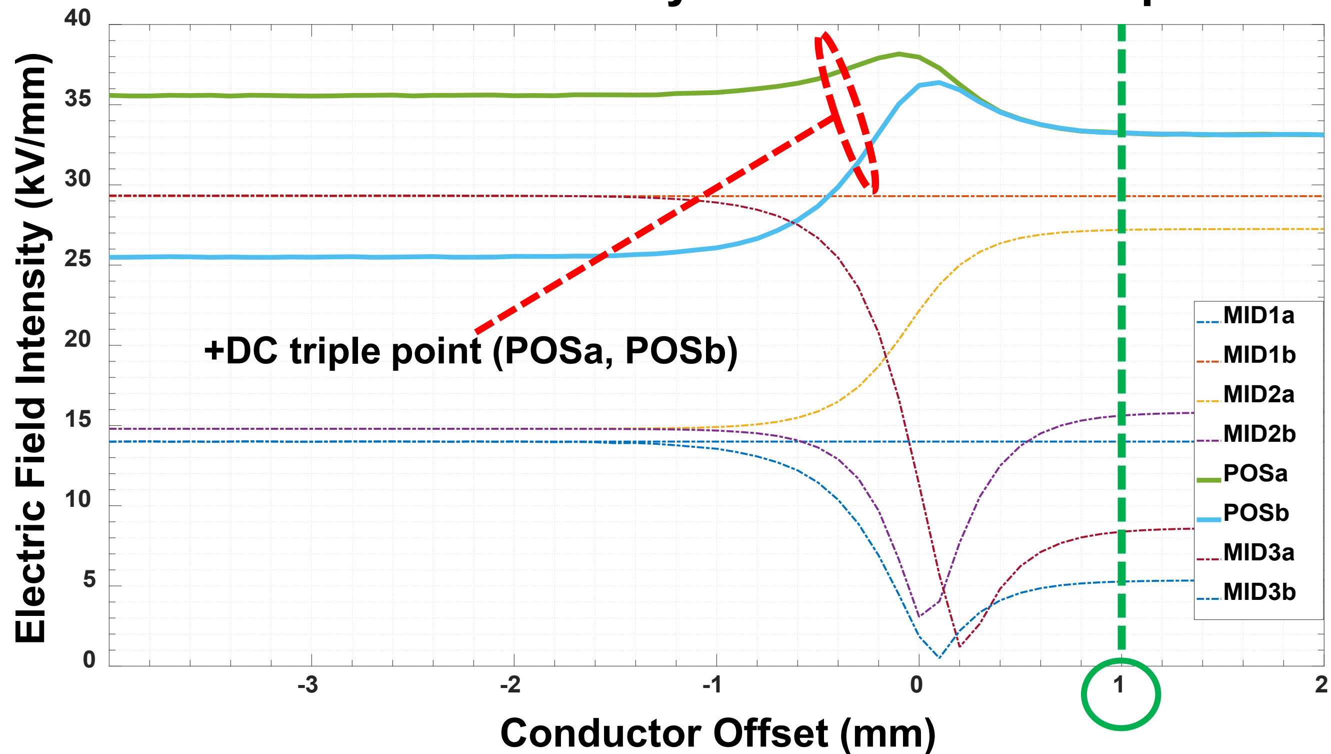


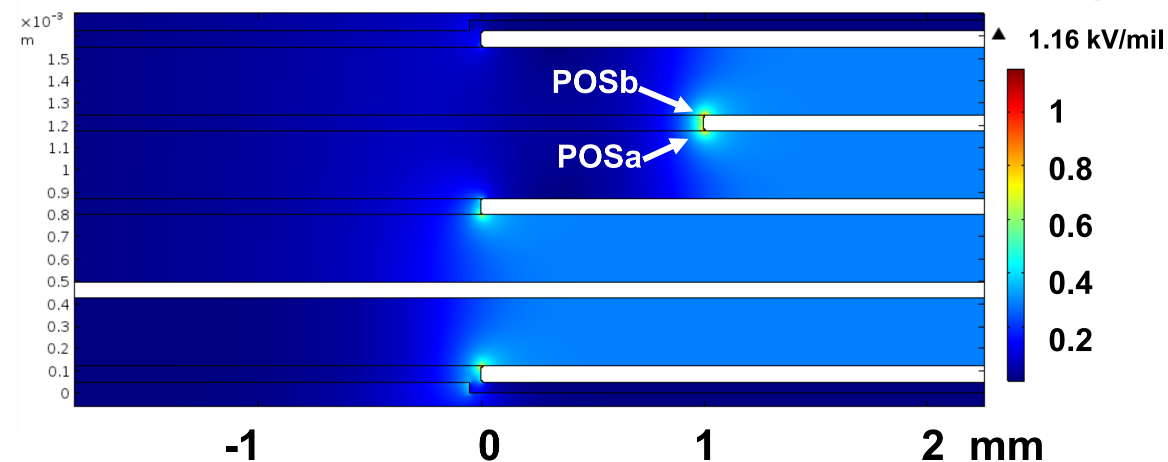


Technique for Electric Field Management within PCB



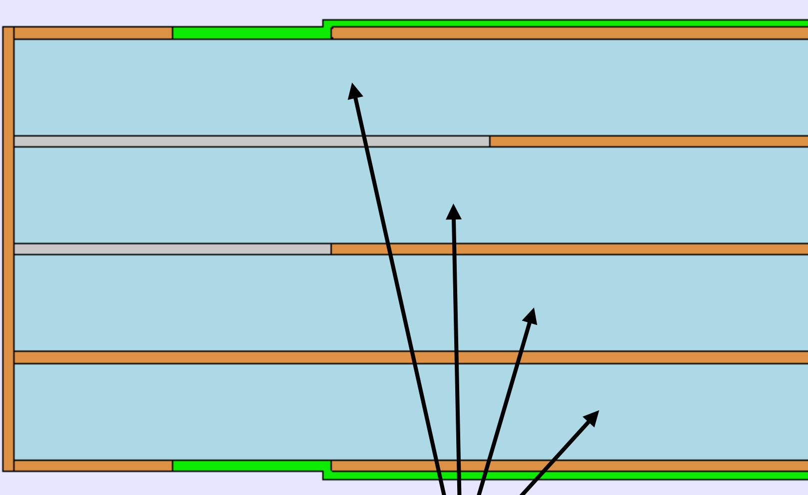




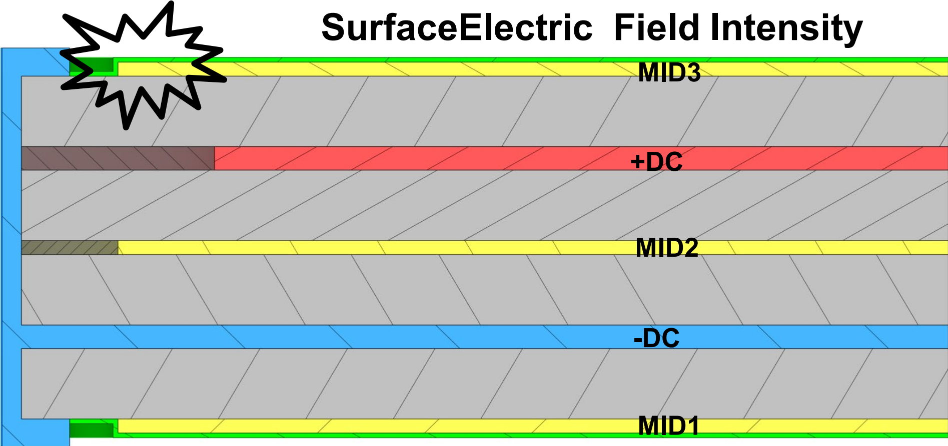


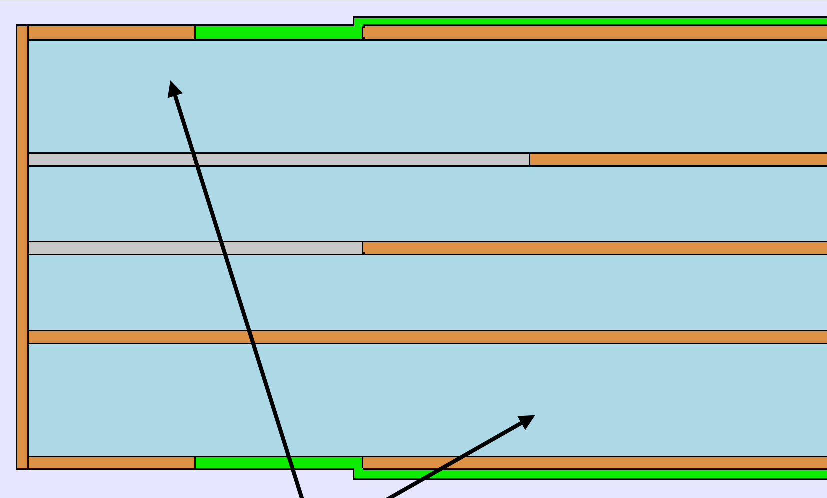
E_{max} reduced 13%

Controlling Surface Electric Field in Air: Techniques



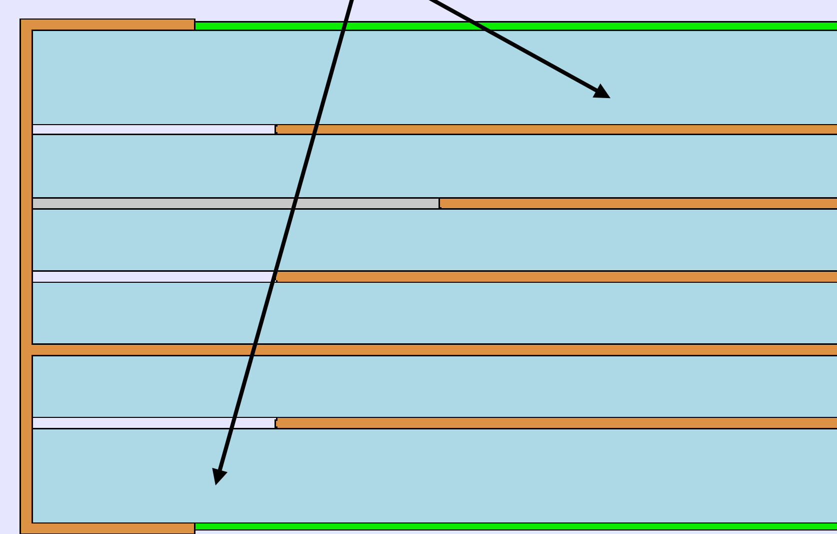
Configuration 1: Additional insulation between all layers



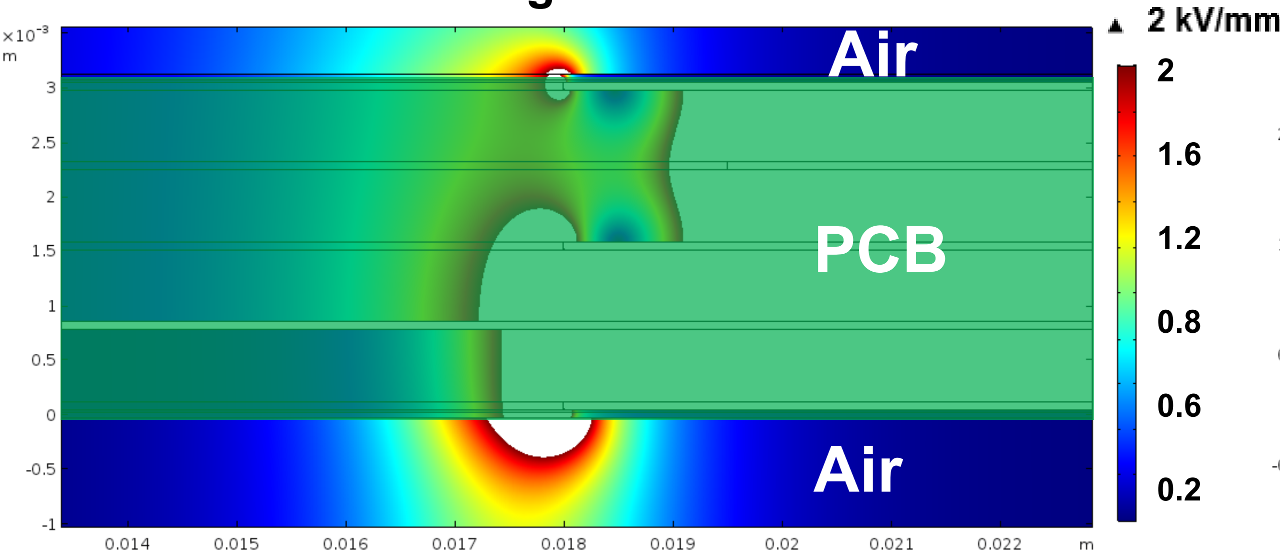


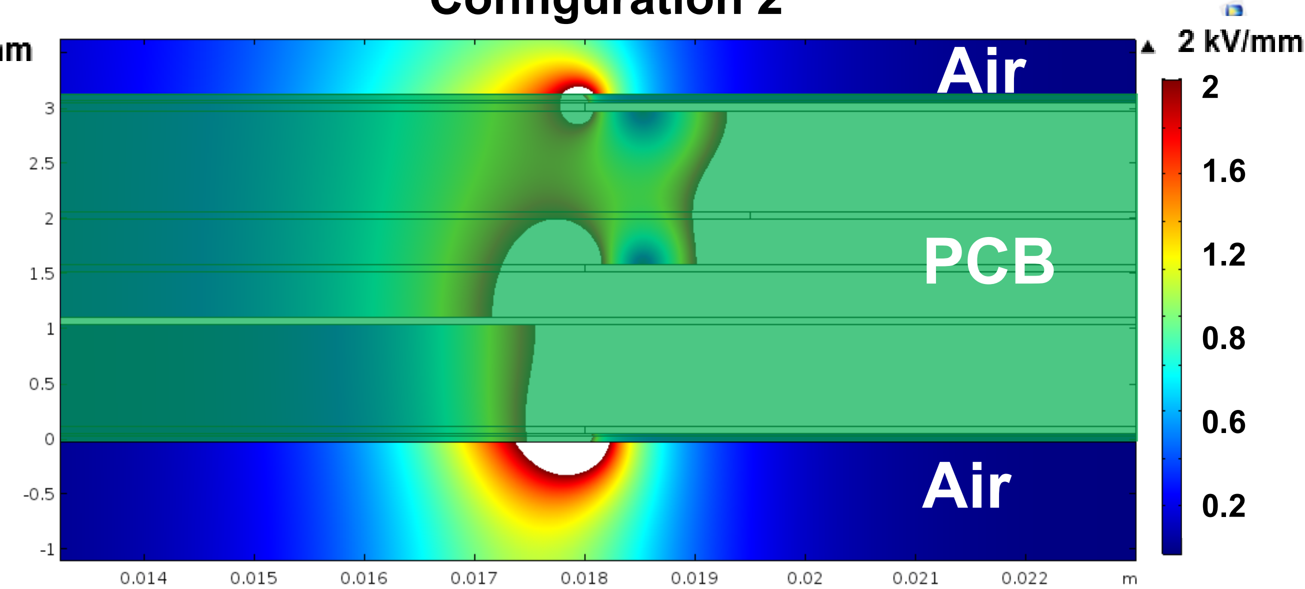
Configuration 2: Additional insulation between outer MID & +/- DC

Configuration 3: Additional outer cores between outer MIDs and air



Controlling Surface Electric Field in Air: Findings



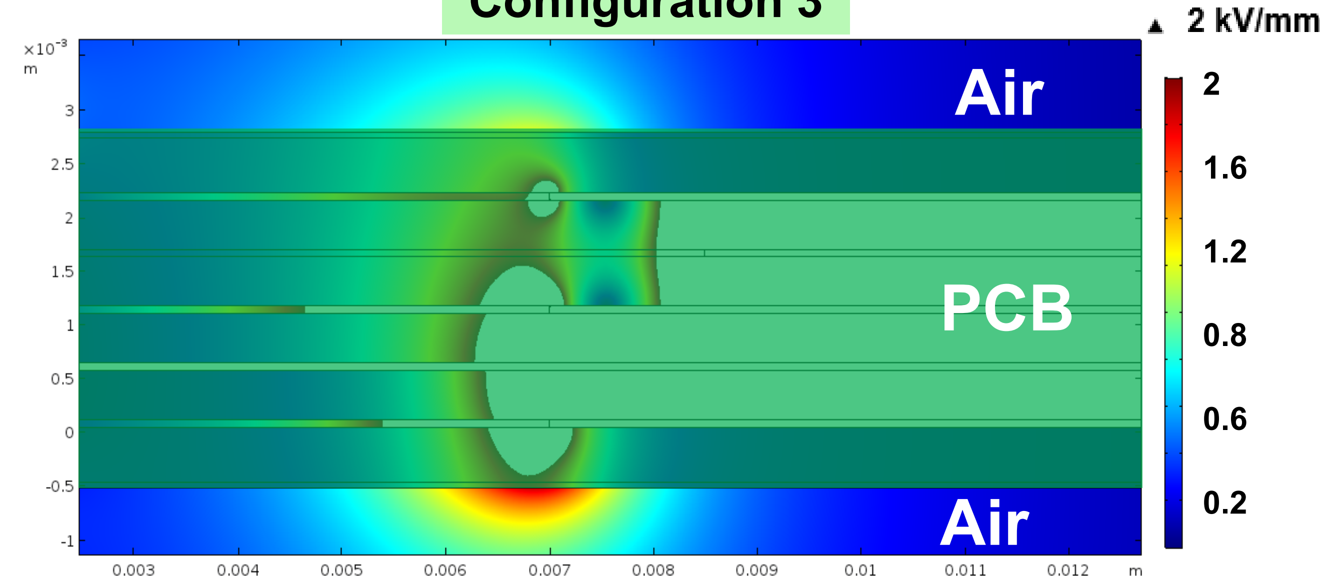


Configuration 1: Additional insulation between each internal layer – 10 mil each

Configuration 2: Additional insulation between two external MID layers – 20 mil each

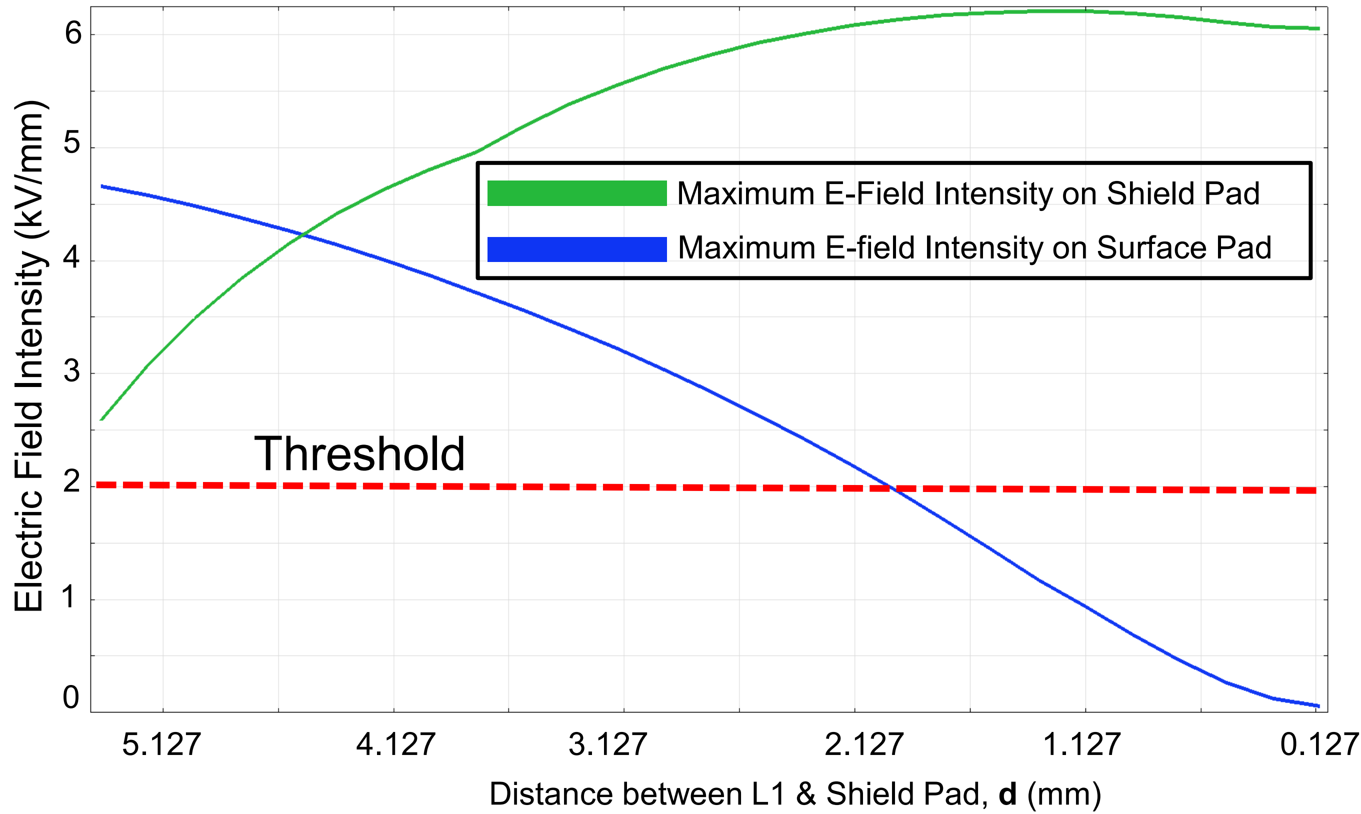
Configuration 3: Additional outer core – 20 mil each

- Green: Region within FR4
- White: E-field intensity >2 kV/mm



Pad Shields & E-Field Control In Air

- 24 kV, 9-Level PCB-bus
- 3 kV between adjacent layers
- "Shield Pads" implemented for surface field control



L1,18 – Component interconnection pads

L2,17 – Internal E-field shielding

Air

Dielectric

Offset

d

24 kV

12 kV

12 kV

0 V

0 V

d

24 kV

12 kV

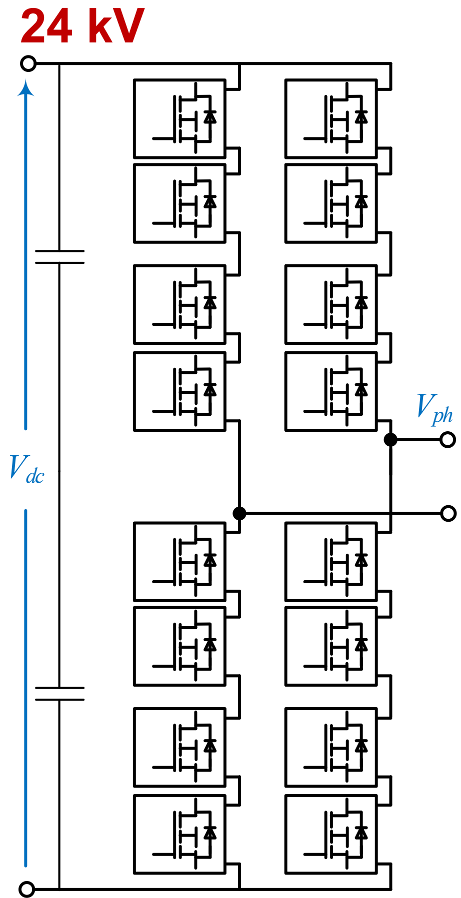
12 kV

0 V

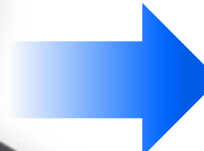
0 V

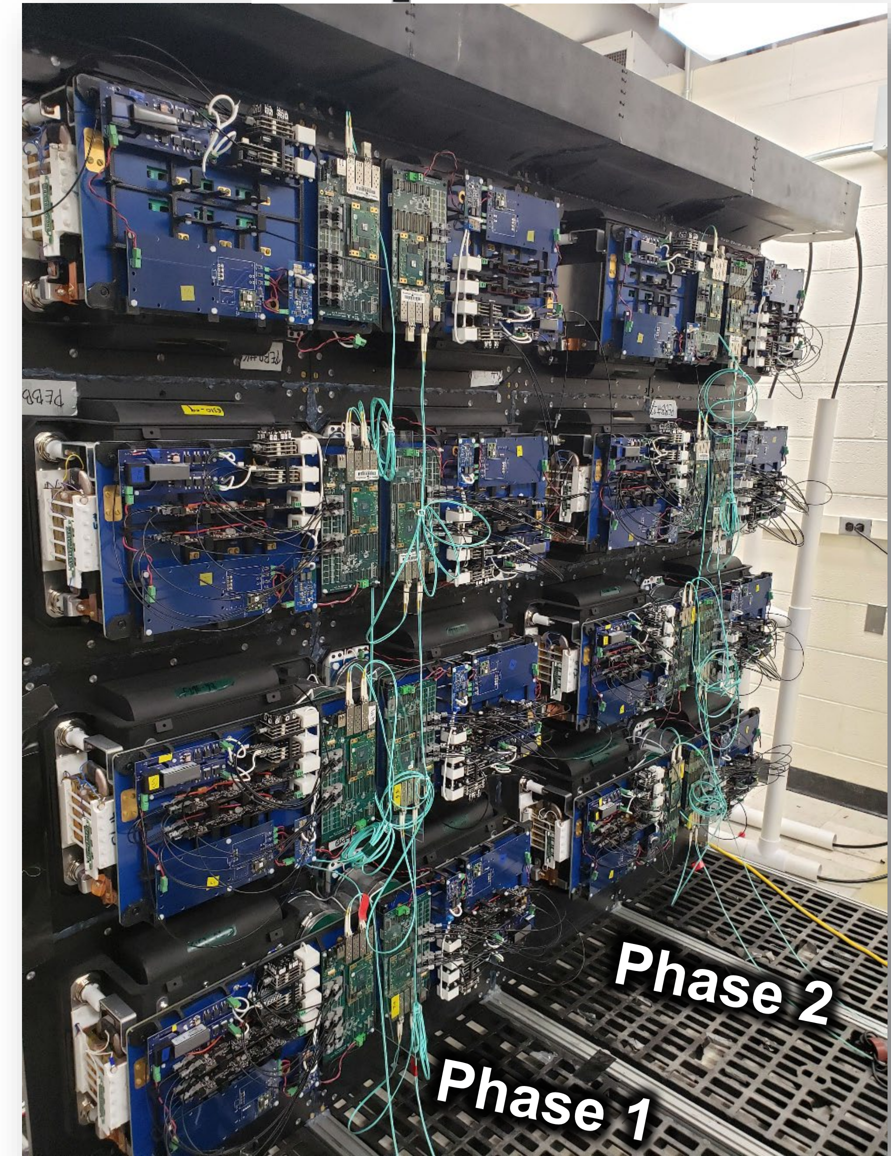
24 kV SiC-based Modular Multilevel Converter

24 kV



dc-dc / dc-ac





Rating = 6 kV, 84 A rms, f_{sw} 10 kHz
PDIV = 32 kV
Power density = 12 MW/m^3
η = 99.4 %

Integrated Auxiliary Power Distribution

- Wire routing throughout converter can be eliminated by integrating low voltage power distribution into 6 kV PCB bus.
  - All ancillary circuits are supplied from 48 V WPT.
    - Additional bus thickness is minimal since differential voltage between MID layer is 48 V
- Four parallel 2 oz layers used for +DC & -DC layers for current carrying capacity
- Independent 48 V layers on top and bottom of bus
  - 48 V input, 48 V distribution

Discrete MVDC Bus

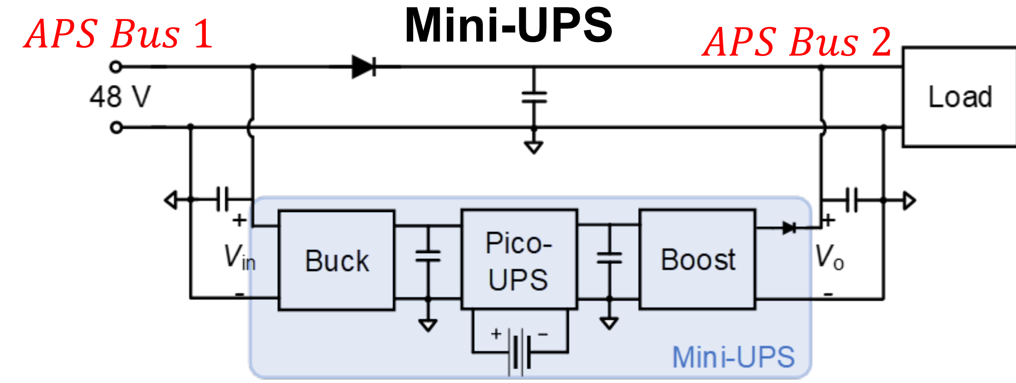
0 V

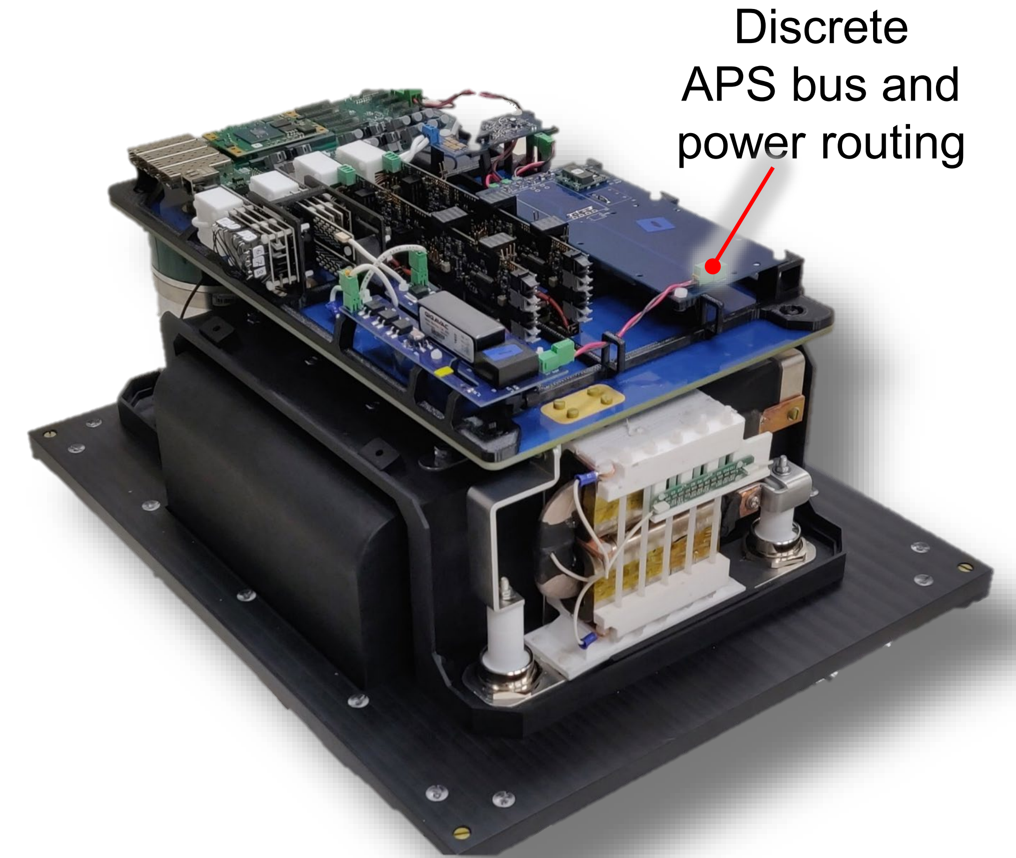
+3 kV

0 V

-3 kV

0 V





CIRCUITS: Half-Bridge 500 kW, 6 kV

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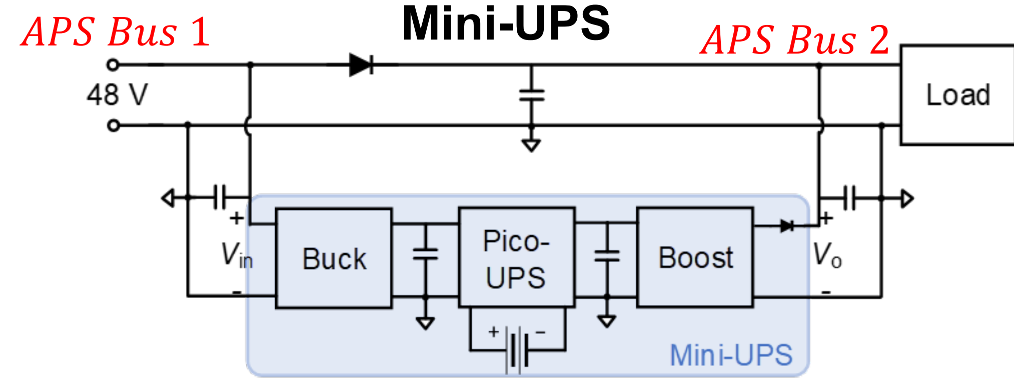
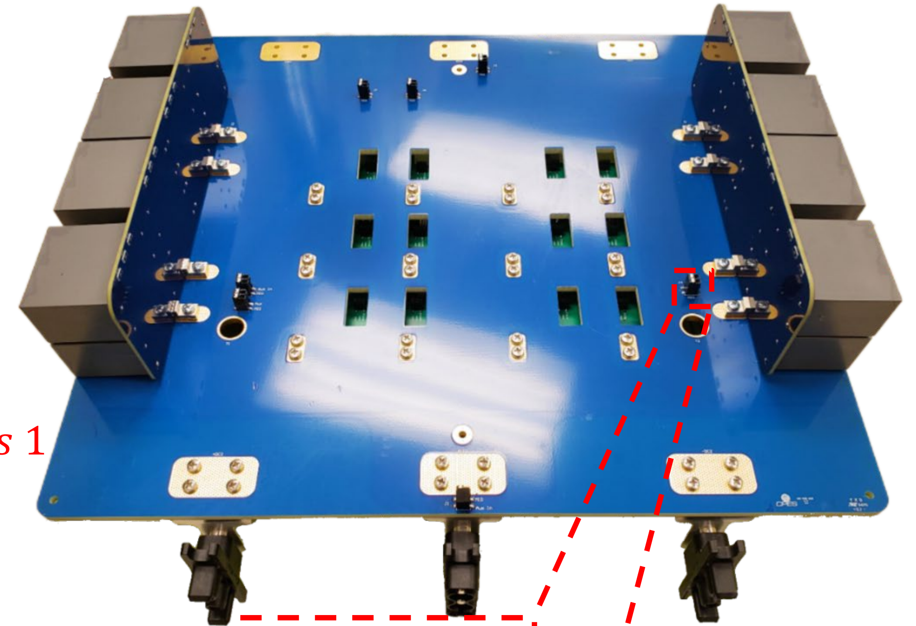
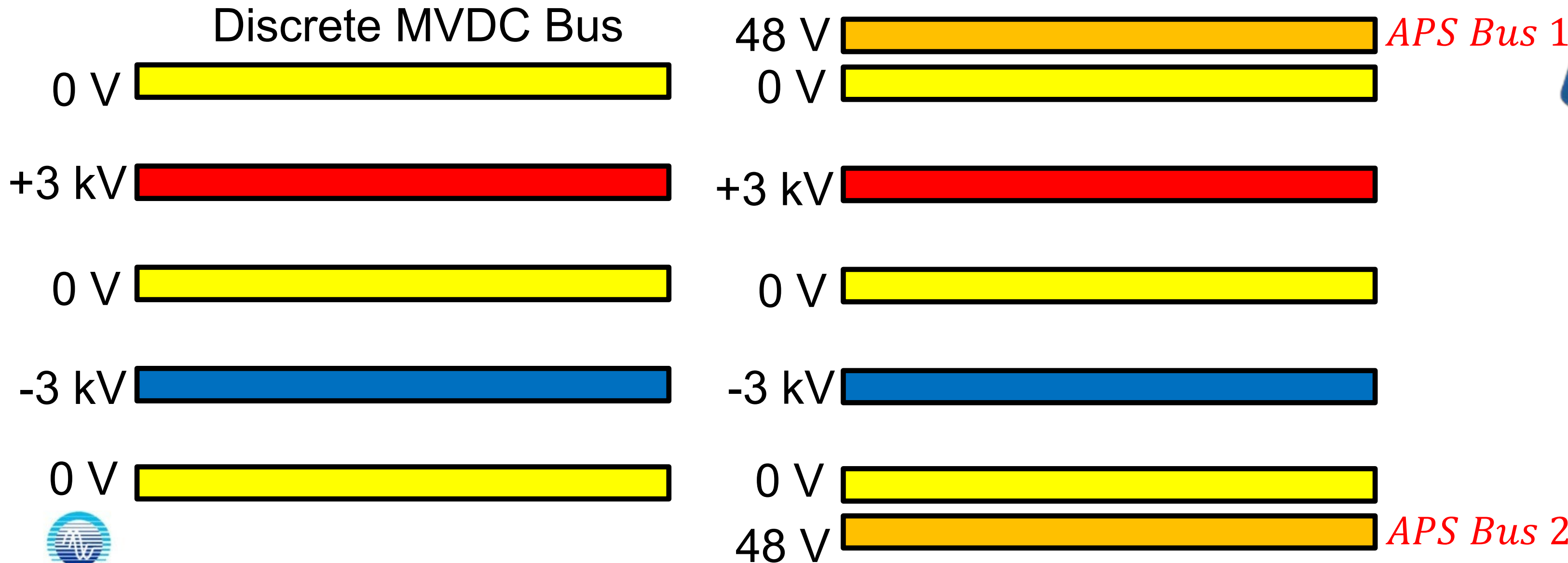


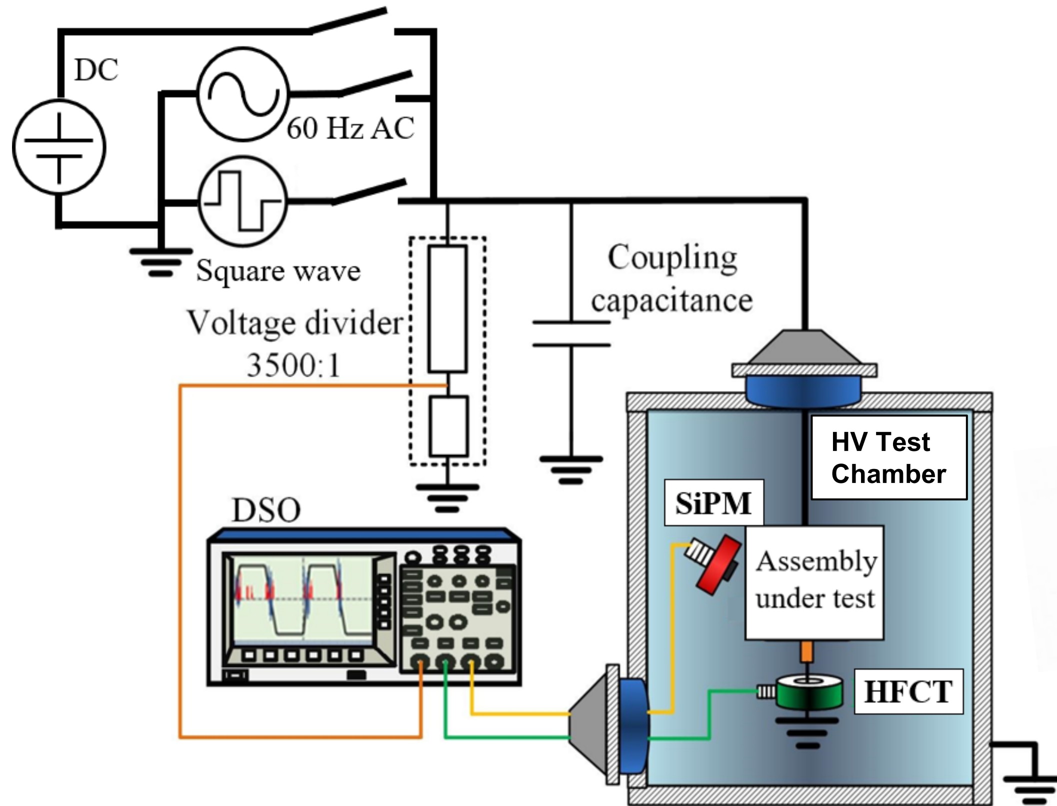


SMD Auxiliary Power Terminals

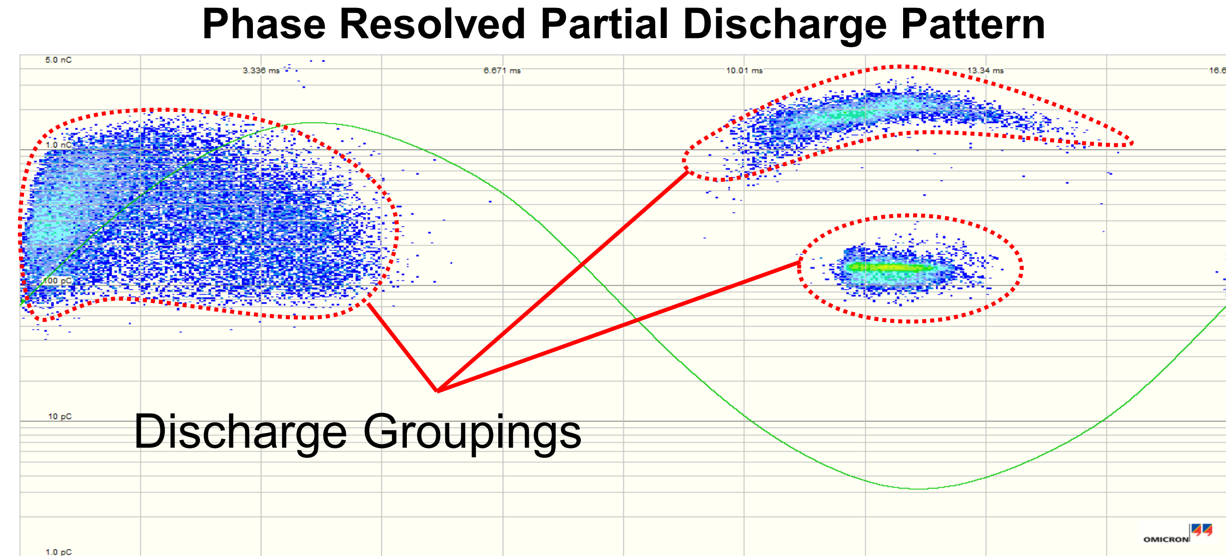


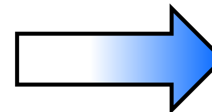
Testbed for Partial Discharge Analysis

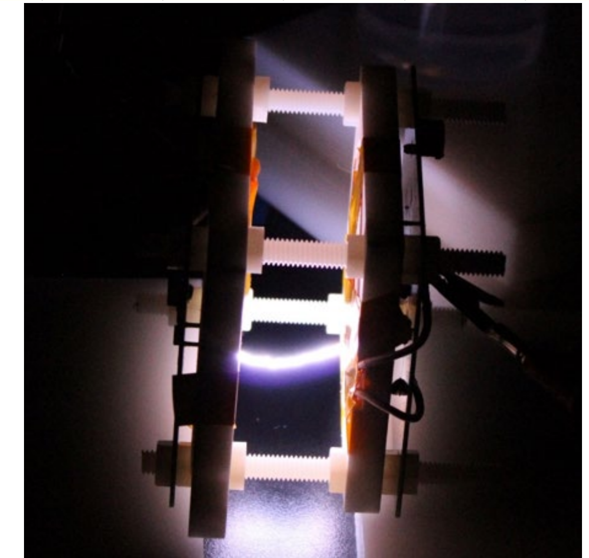
- Omicron partial discharge measurement system for detecting and analyzing partial discharge events
- Canon DSLR for capturing flashover and corona on parts exposed to air



Phase Resolved Partial Discharge Pattern



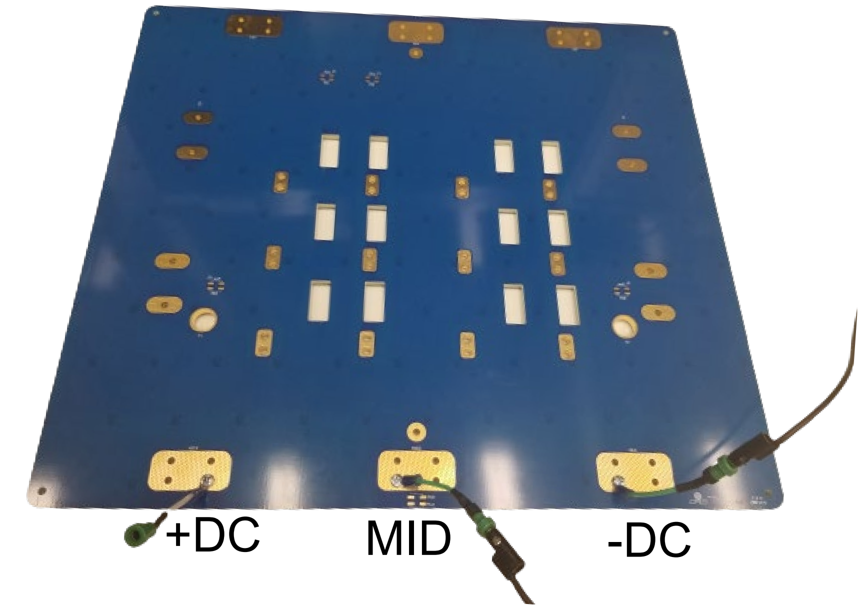


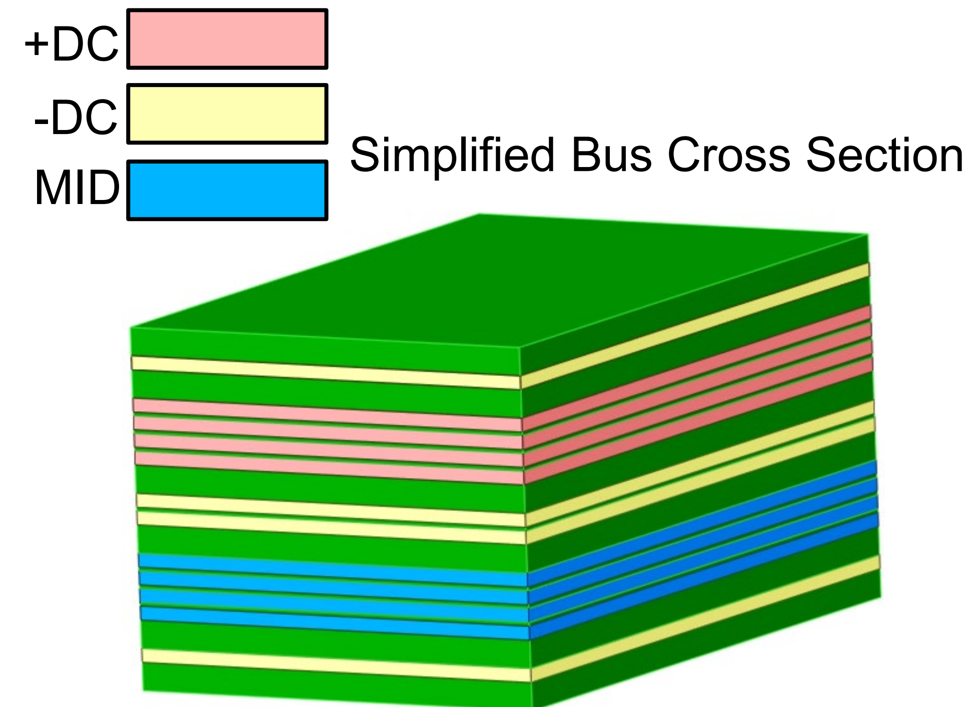


Flashover Between HV Coils

Bus Insulation Performance: PD Inception Voltage (PDIV)

- Insulation between +DC, -DC, and MID tested with 60 Hz AC excitation
- PDIV target > 3.6 kV between Mid & ±DC with apparent charge < 10 pC
- PCB bus weight is 6 lb – reduced by 66%





Connection				PDIV (kV)
	High Voltage	Reference	Floating	
1	+DC	-DC/MID	—	6.4
2	-DC	+DC/MID	—	6.33
3	+DC/-DC	MID	—	6.48
4	+DC	-DC	MID	8.12
5	+DC	MID	-DC	6.87
6	-DC	MID	+DC	6.80

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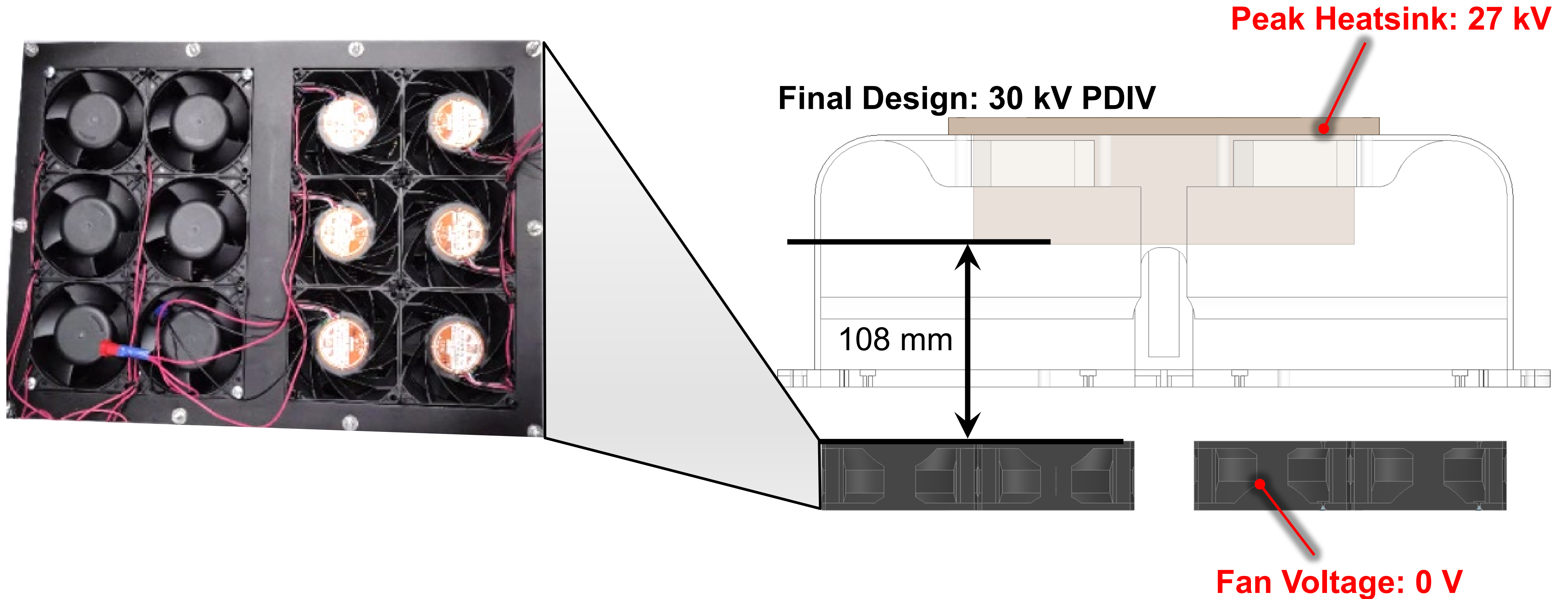
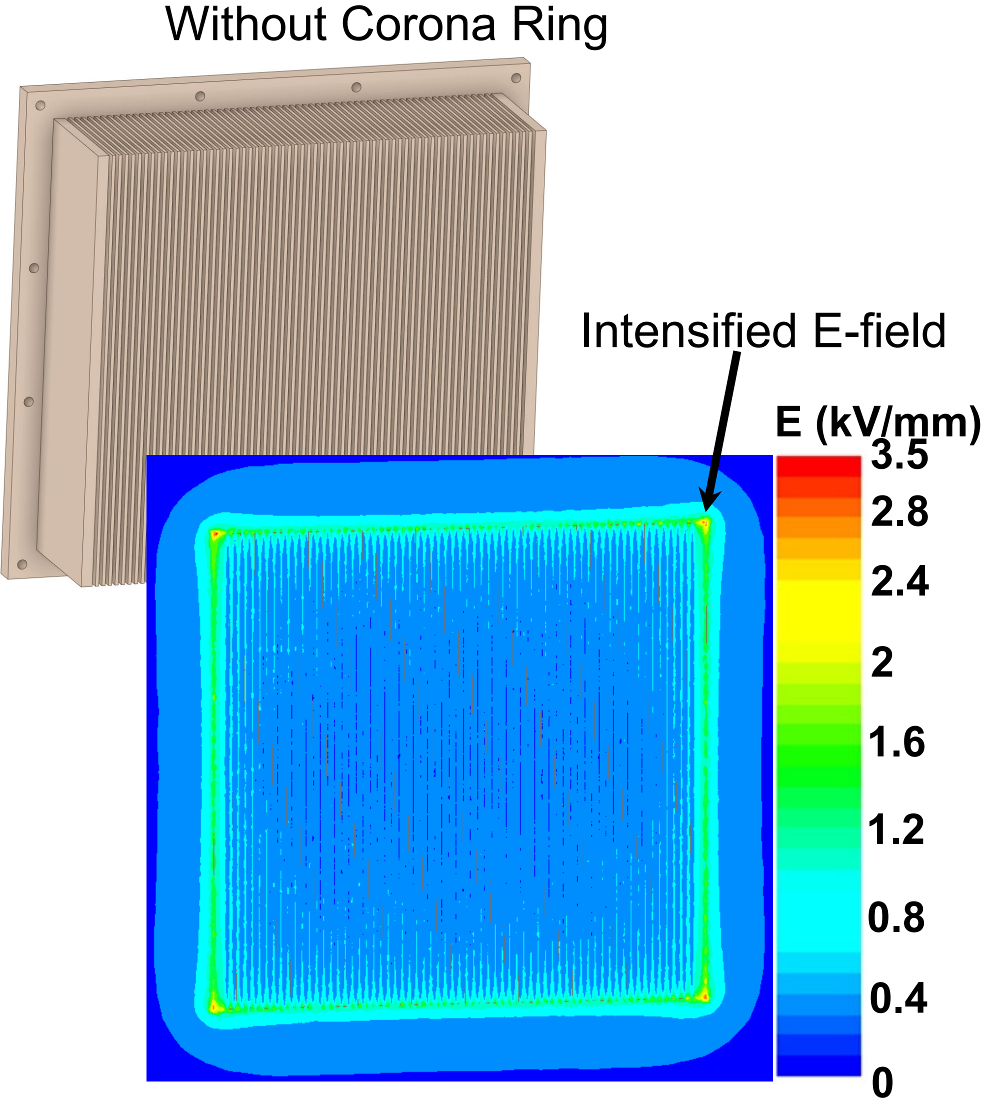
Cooling System Insulation Challenges

- Clearance requirement in air is increased due to non-ideal geometries within cooling system
  - Sharp edges along heatsink
  - Internal electronic circuitry of fan array



Electric Field Reduction Using Corona Ring



With Corona Ring

Tube radius R_t

Corner radius R_r

Horizontal location L_H

Vertical location L_V

Horizontal location L_H

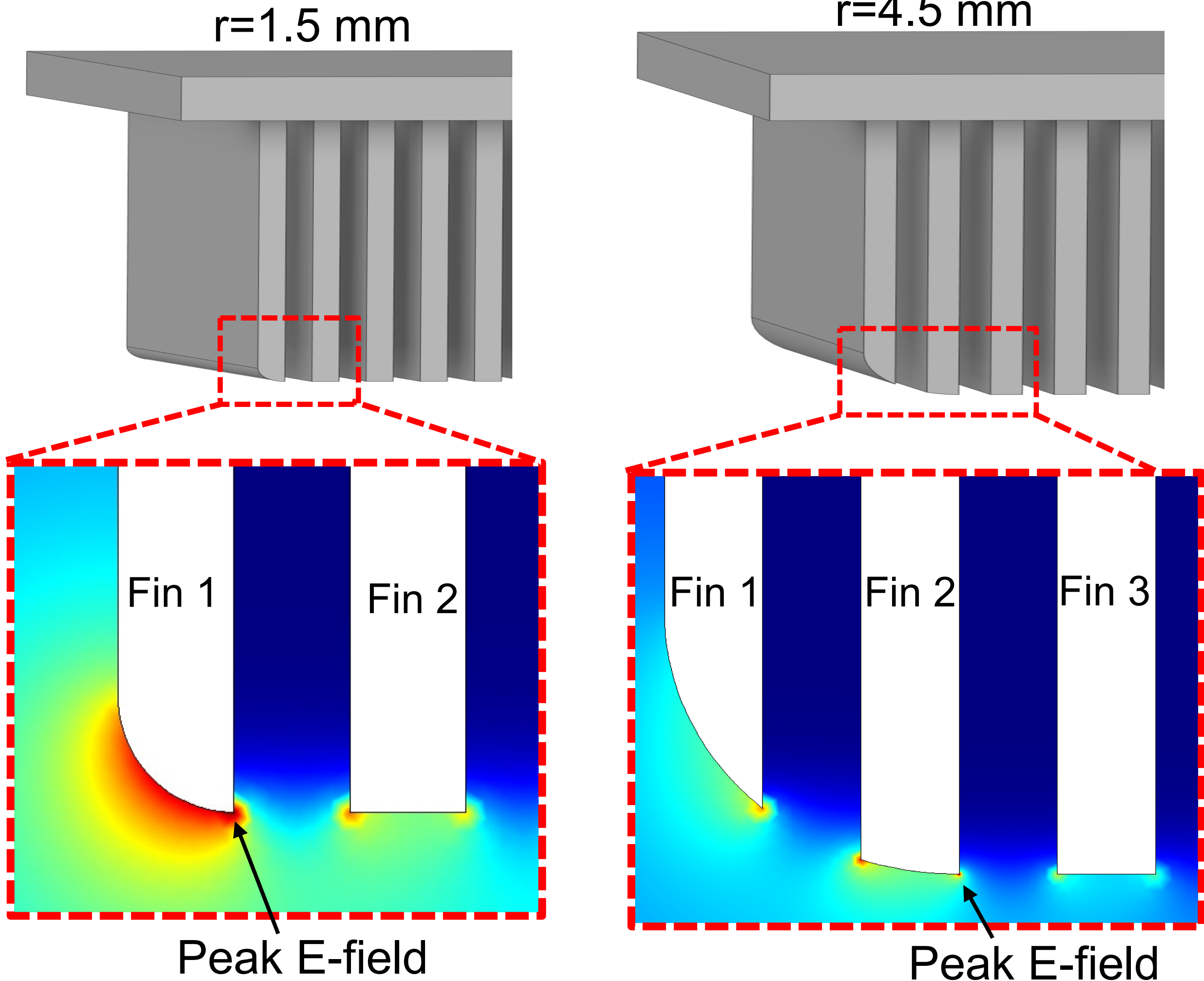
Smoothed E-field

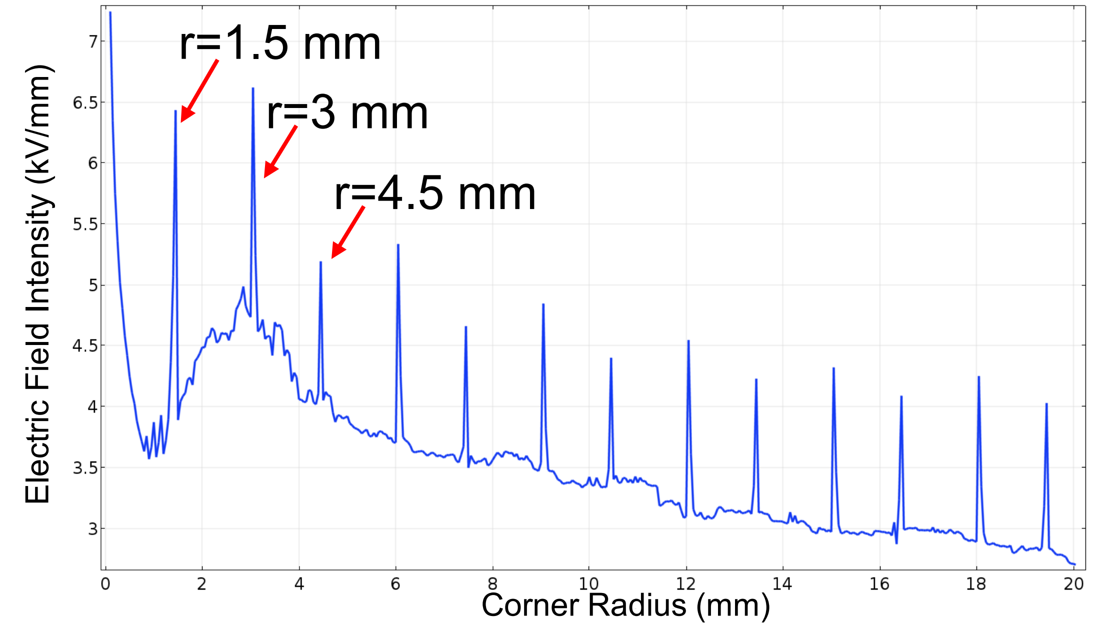
E (kV/mm)

3.5
2.8
2.4
2
1.6
1.2
0.8
0.4
0

- Peak E-field intensity reduced by ~50 %

E-field Reduction on Edge 1





- Fin "Knife edge" must be avoided to prevent E-field intensification.

Design Guide:

If $w = s$

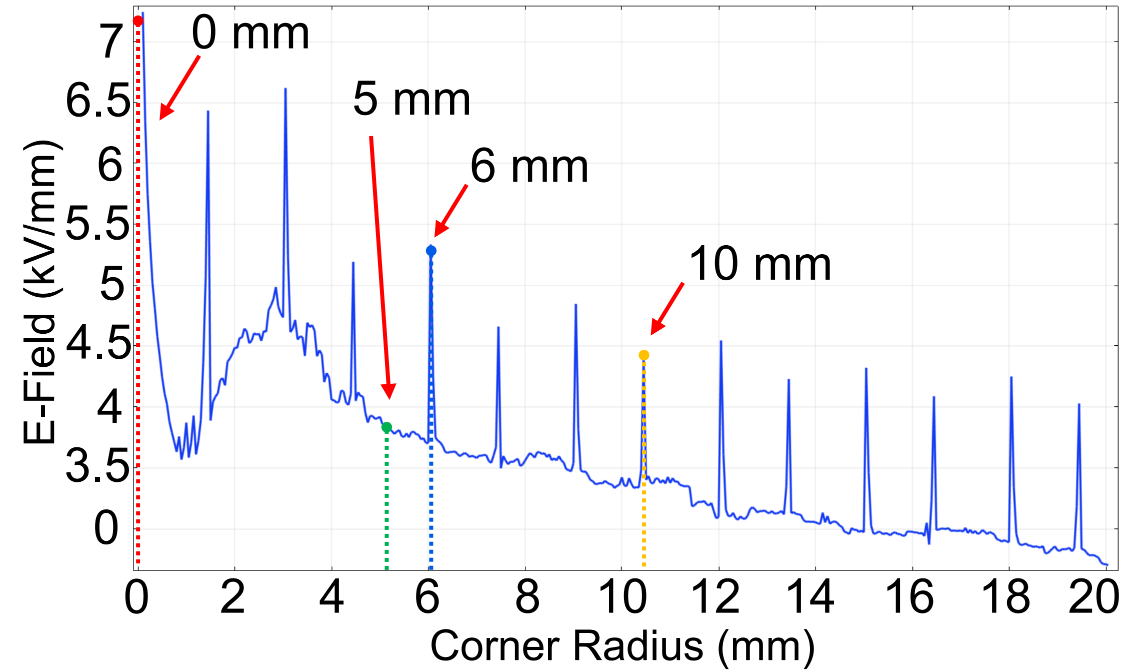
$r \neq nw$

If $w \neq s$

for $r > w$

$r \neq n(w + s)$

High Voltage Heatsink Validation



Heatsink Coupon PDIV

Radius (mm)	PDIV (kV)	Change (%)
0	12.48	—
5	16.97	+36
6	14.68	+18
10.5	14.58	+17

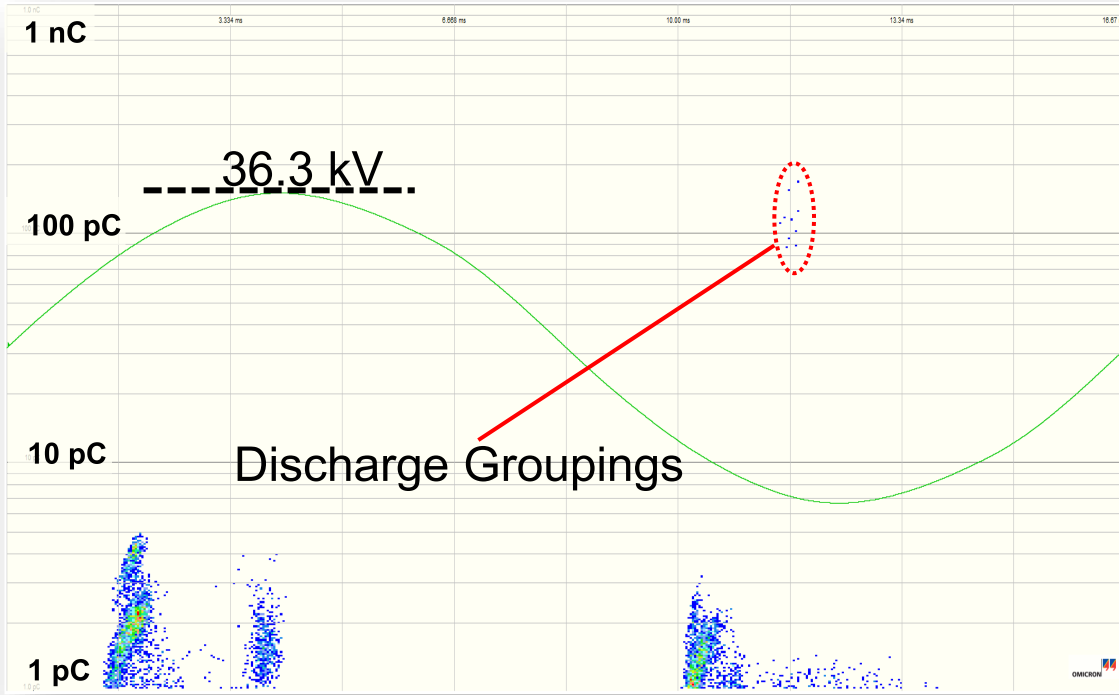
Design Guide:
If $w = s$
$r \neq ns$

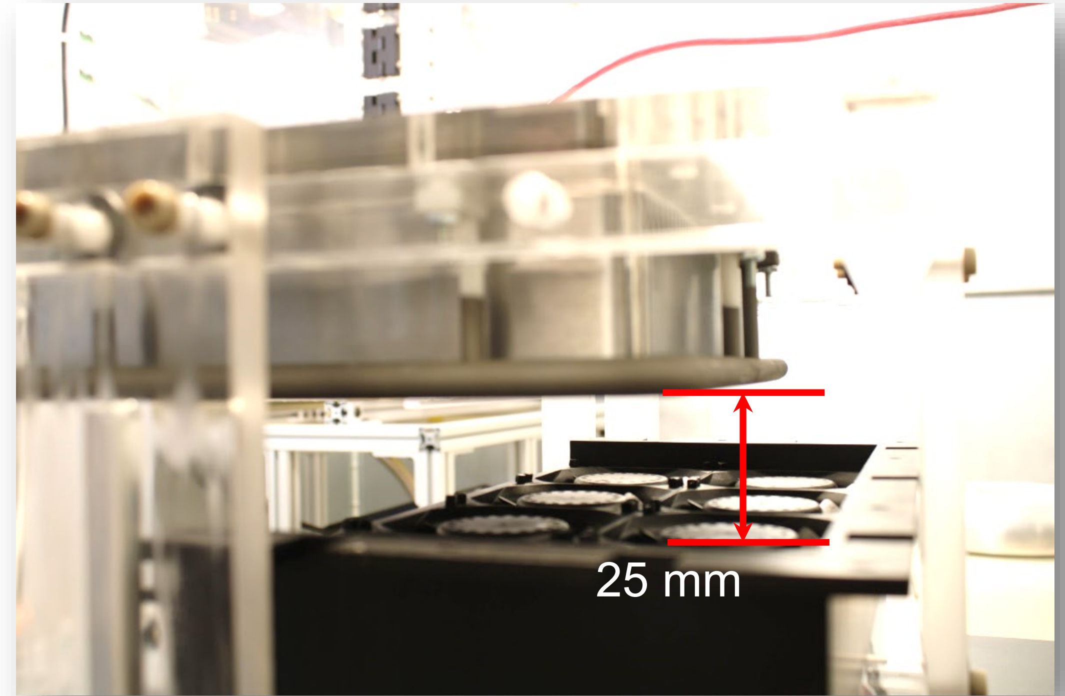
If $w \neq s$
for $r > w$
$r \neq n(w + s)$

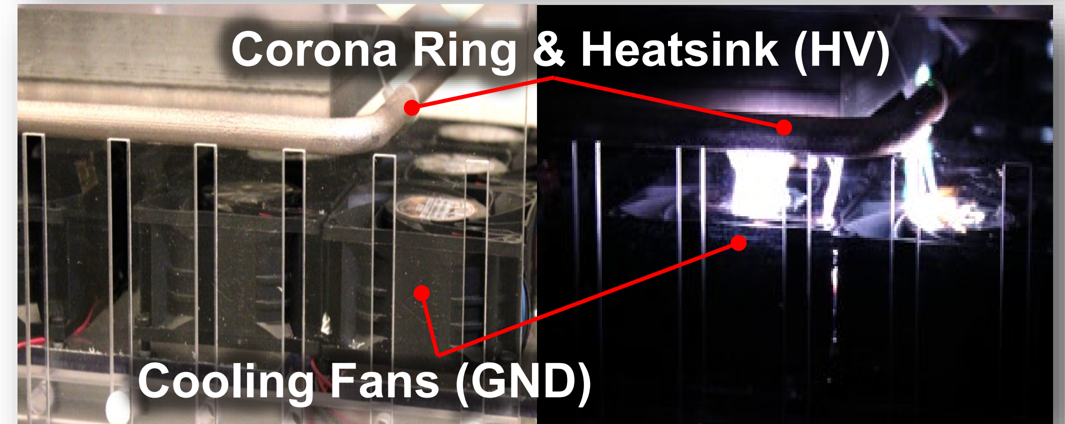
$r = 6\,mm$ $r = 10.5\,mm$
$r = 0\,mm$ $r = 5\,mm$

Heat Sink-to-Fan Insulation Testing

PRPD: Heatsink-to-Fans







- Fan clearance reduced to 25 mm
- Spacer with height of 25 mm was used to set spacing between corona ring and top of fans
- PDIV = 36.3 kV
- Flashover Voltage: 49.2 kV

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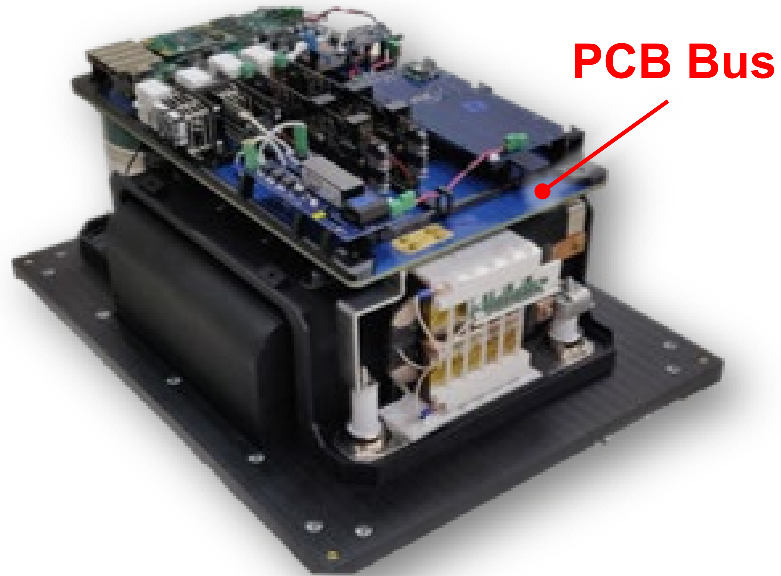
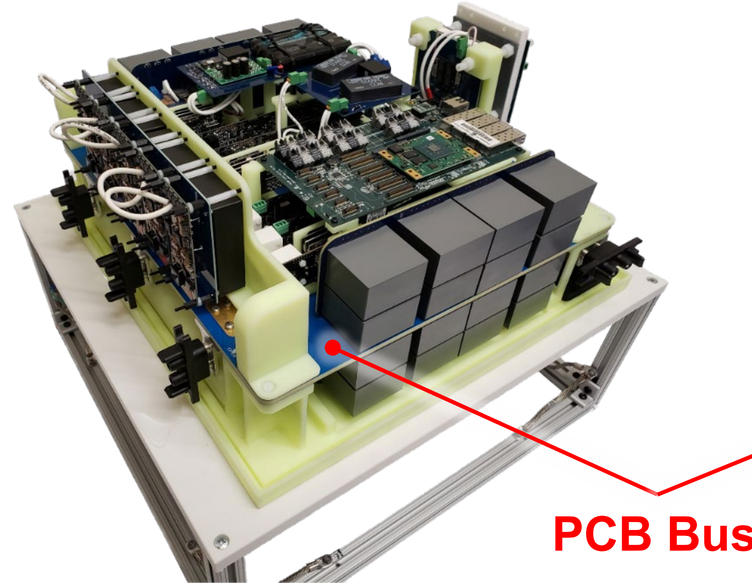
Medium Voltage Converters at CPES Utilizing PCB-Based Bus

ARAP-E: CIRCUITS



Topology	Half-Bridge
Voltage	6 kV
Current	83 A
Power	500 kW
Frequency	10 kHz
Efficiency	99.4%
Power Density	12 MW/m^3 (197 w/in^3)

ONR: PEBB 6000



Topology	H-Bridge
Voltage	6 kV
Current	176 A
Power	1 MW
Frequency	10 kHz
Efficiency	99.4%
Power Density	20 MW/m^3 (327 w/in^3)

AMMTO (AMO)

Topology	5-Level Flying Capacitor
Voltage	22 kV
Current	15 A
Power	333 kW
Frequency	5 k
Efficiency	TBD
Power Density	2.8 MW/m^3 (46 w/in^3)

Concluding Remarks

- Implementing geometric techniques for E-field control enables use of MV PCB-based components.
- MV PCB-based DC bus with integrated low voltage network simplified insulation system of PEBB structure
- PCB bus was designed to successfully reach target PDIV of 8.12 kV with a weight reduction of 66%
- PCB-based 3 kV, 44 μF capacitor daughtercards with integrated balancing resistors eliminated the need for MV can-type capacitors
- The use of a corona ring and rounded heat sink reduced distance between fan array and heatsink by 75%
- **Power density increased by 48%**

Thanks!

Please contact me anytime at joshstew@vt.edu

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