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Packaging and Integration Design for High-Voltage WBG Modules

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Spellman High Voltage Power Electronics Lab

Stony Brook University

2023 Power Electronics and Energy Conversion Workshop

Aug 3,2023

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Spellman HV Power Electronics Lab

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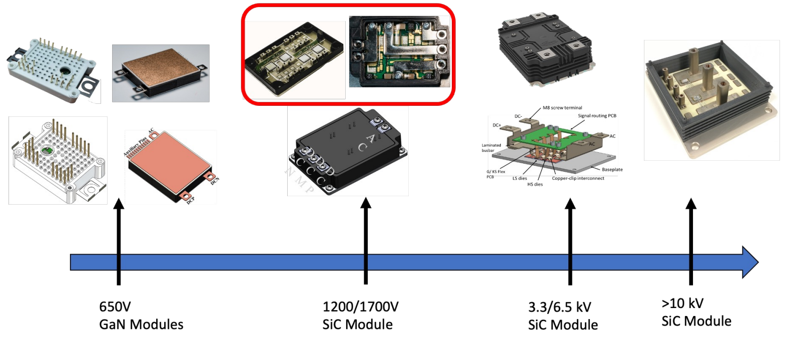
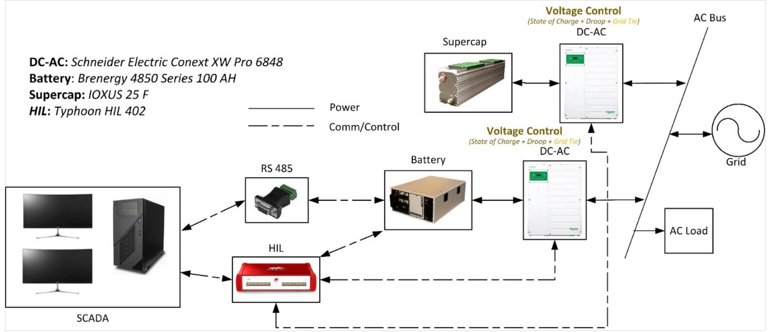
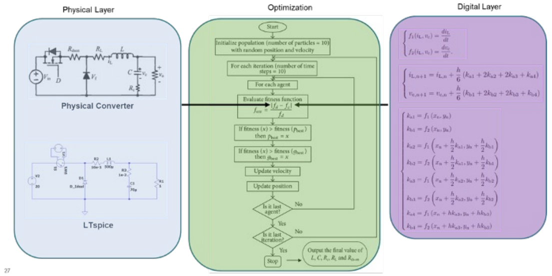
Power Module Packaging



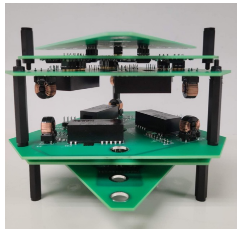


Microgrid PHIL Platform with Hybrid Energy Storages

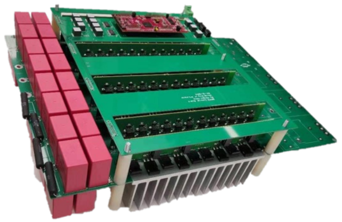


Realtime Digital Twin for Prognostic Diagnostic and Lifetime Managment

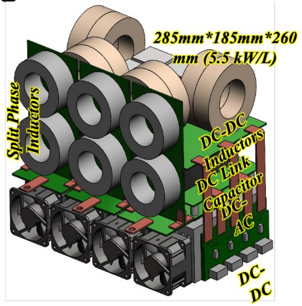
High Performance Power Converters



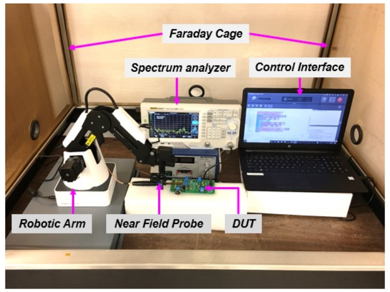
20 kW Cryogenic High Density Motor Drive (GaN)



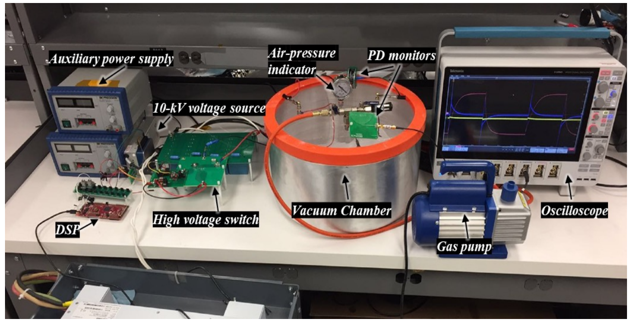
High Density Grid Tied Solar Converter (SiC)



Modular Grid-tied Converter for Grid Control (SiC)



EMI and Reflected Wave in Flying Microgrid/ Active Filtering



High Attitude Partial Discharge Testing and Modeling

Sponsors:

GE Aviation, APEX Microtechnology, Federal Aviation Administration, U.S. Department of Energy, Spellman High Voltage Electronics Corporation, NASA, Raytheon Technologies, GE Research, DARPA, HESSE Mechatronics, NSF, Office of Naval Research Science & Technology

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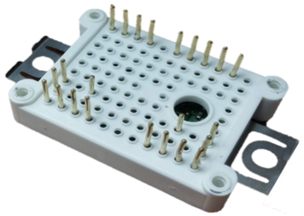
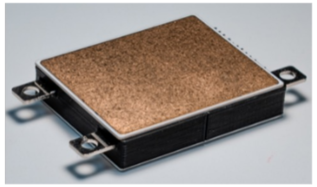
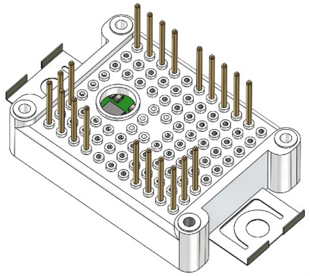
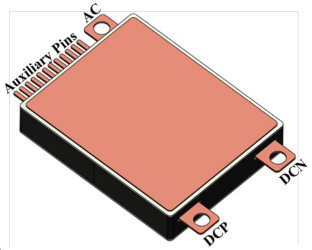
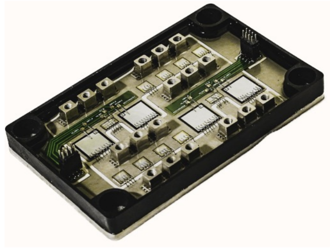
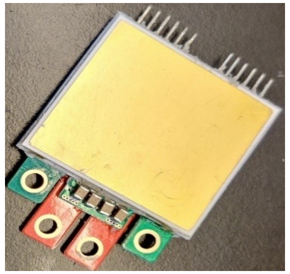
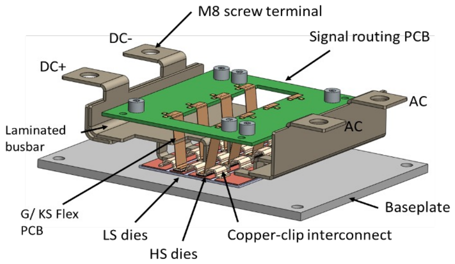
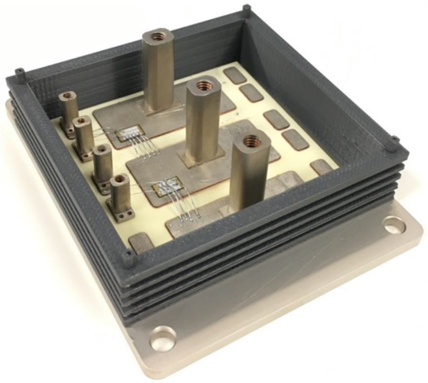
Recent Module Development in the Lab





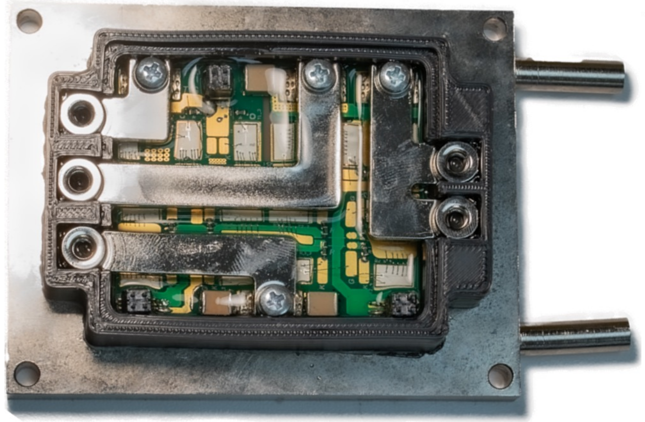
650V
GaN Modules

1200/1700V
SiC Module

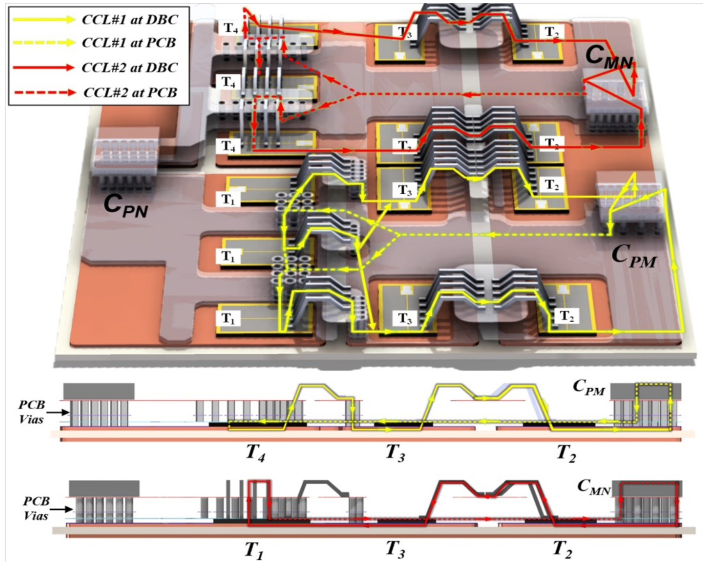
3.3/6.5 kV
SiC Module

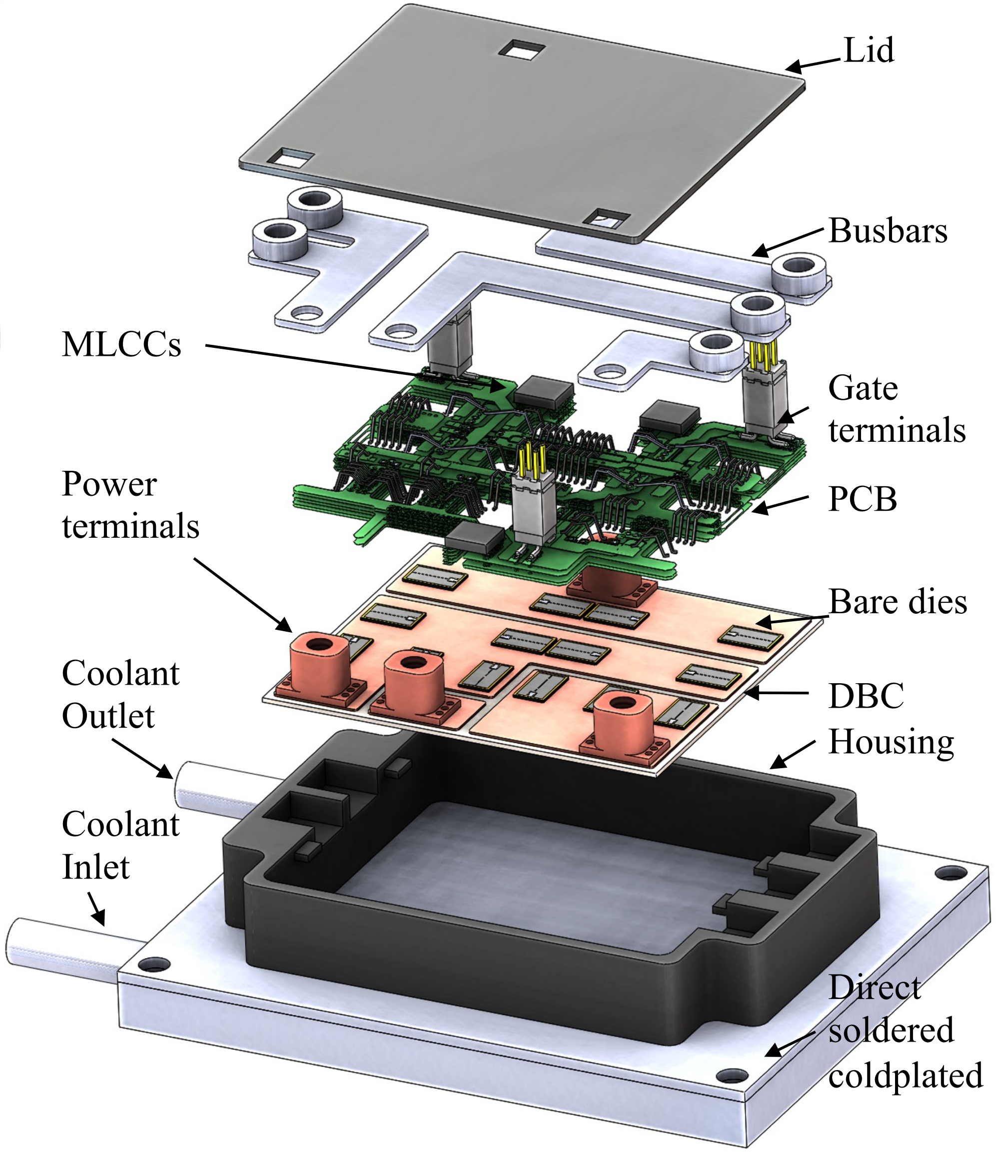
>10 kV
SiC Module

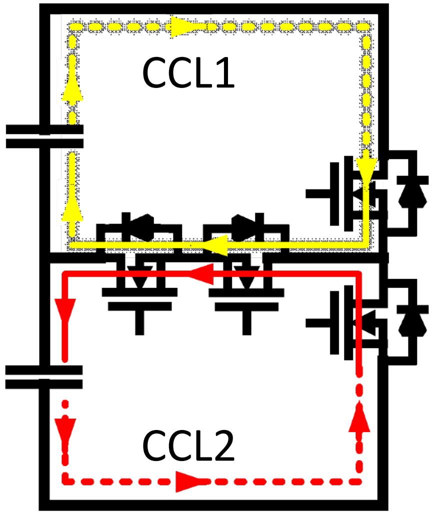
1.2 kV/ 300A 3L-TNPC H^2 Module



Fabricated power module w/o. lid



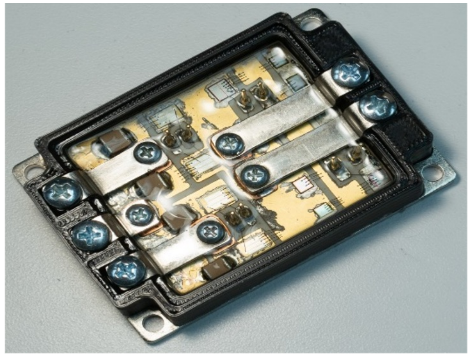


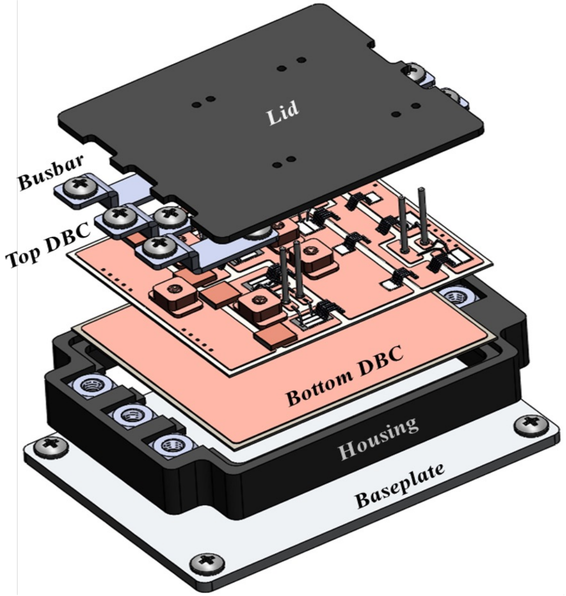


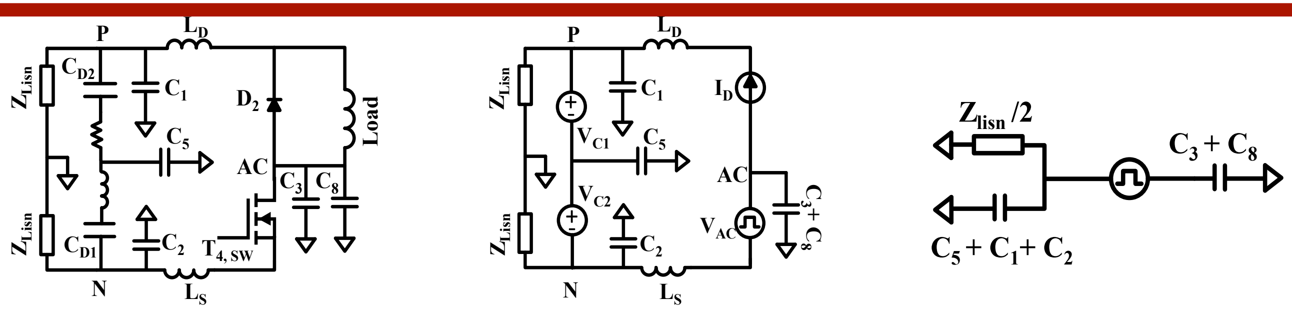
CCLs in 3L-TNPC

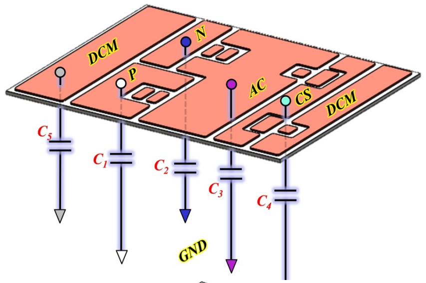
CCL	P-M
CCL1 (P-M)	2.46 nH
CCL2 (M-N)	2.47 nH

1.2 kV/ 150A 3L-TNPC Low EMI Module

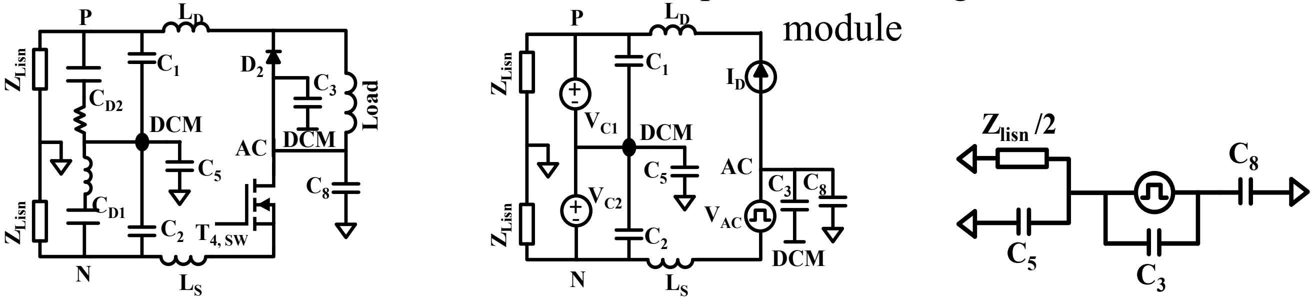


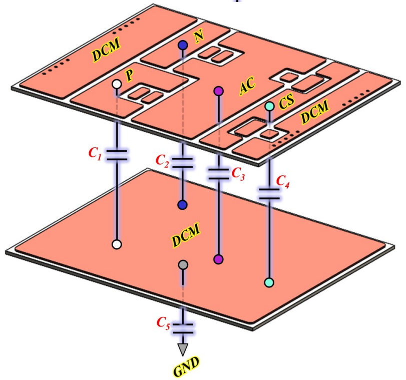




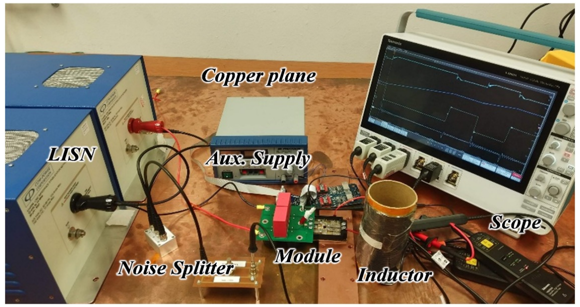


CM Equivalent for single DBC module

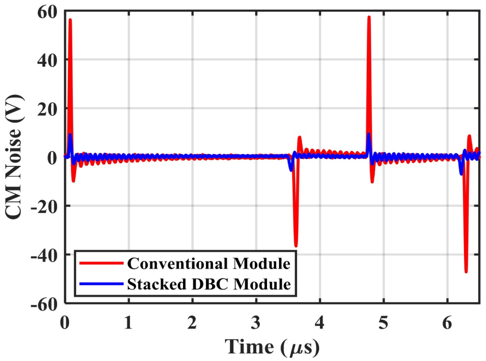




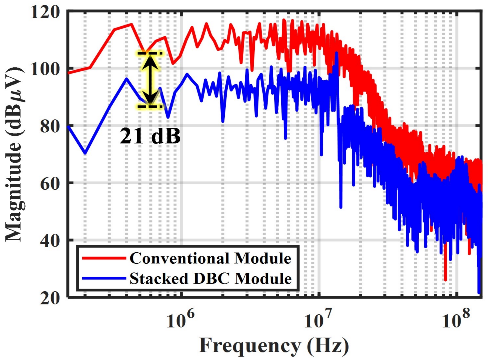
CM Equivalent for stacked DBC module



Test setup: Measurement of CM EMI noise

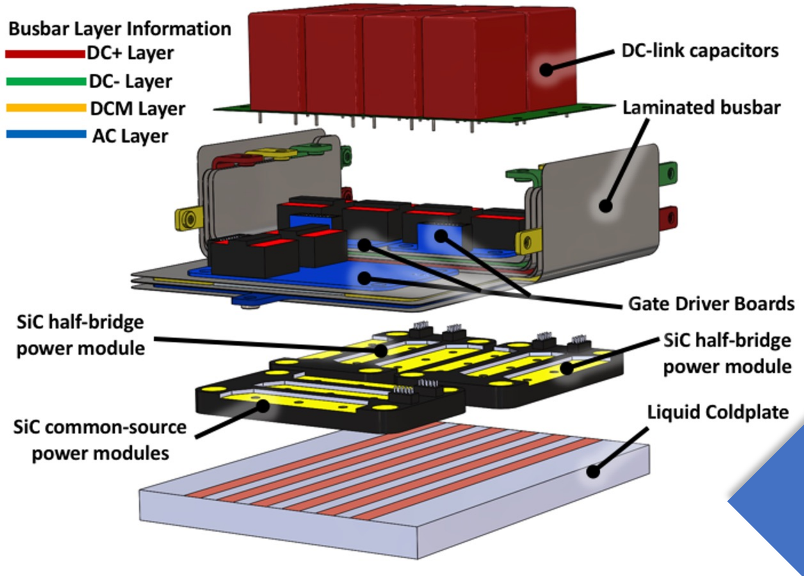


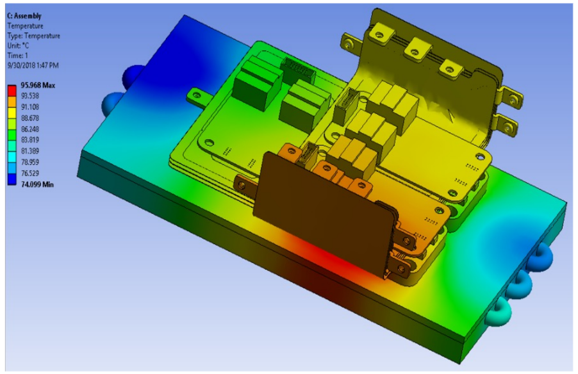
Time-domain result



Frequency-domain result

Co-optimized Thermal Solution for Less-EMI

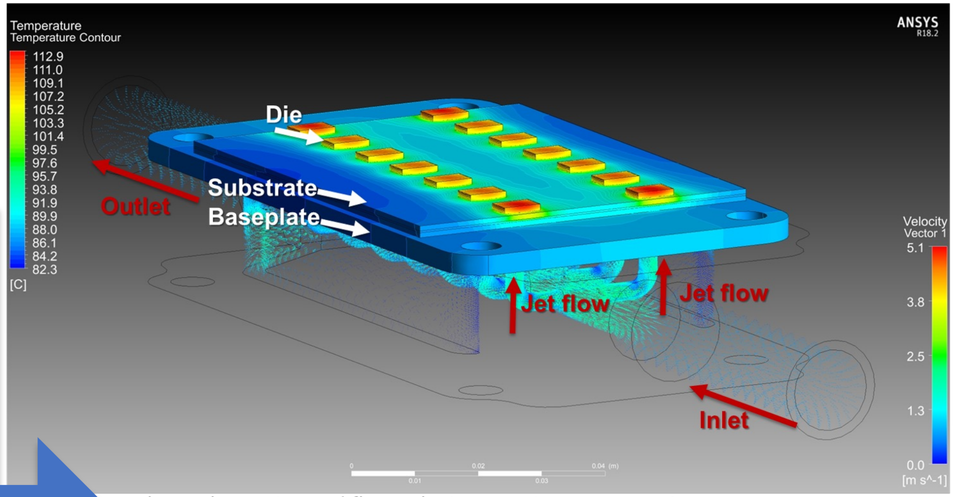




Temperature distribution, 150 kW, 1 GPM @ 70 °C

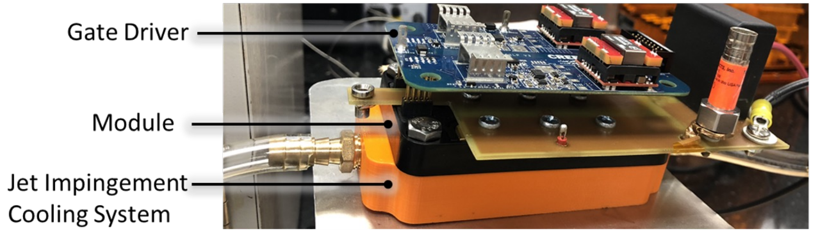
Traditional

Advanced

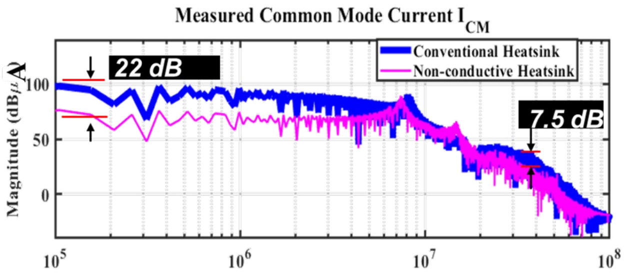


Thermal mapping and flow velocity mapping, 1.5 GPM @ 70°C

3D Printed Non-metallic coldplate



Test Setup ($R_{G,ON}$ = 5 Ω, $R_{G,OFF}$ = 2.5 Ω)



- **Optimized Jet-Impingement coldplate**
- **3D Printed with non-metallic material for EMI optimization**

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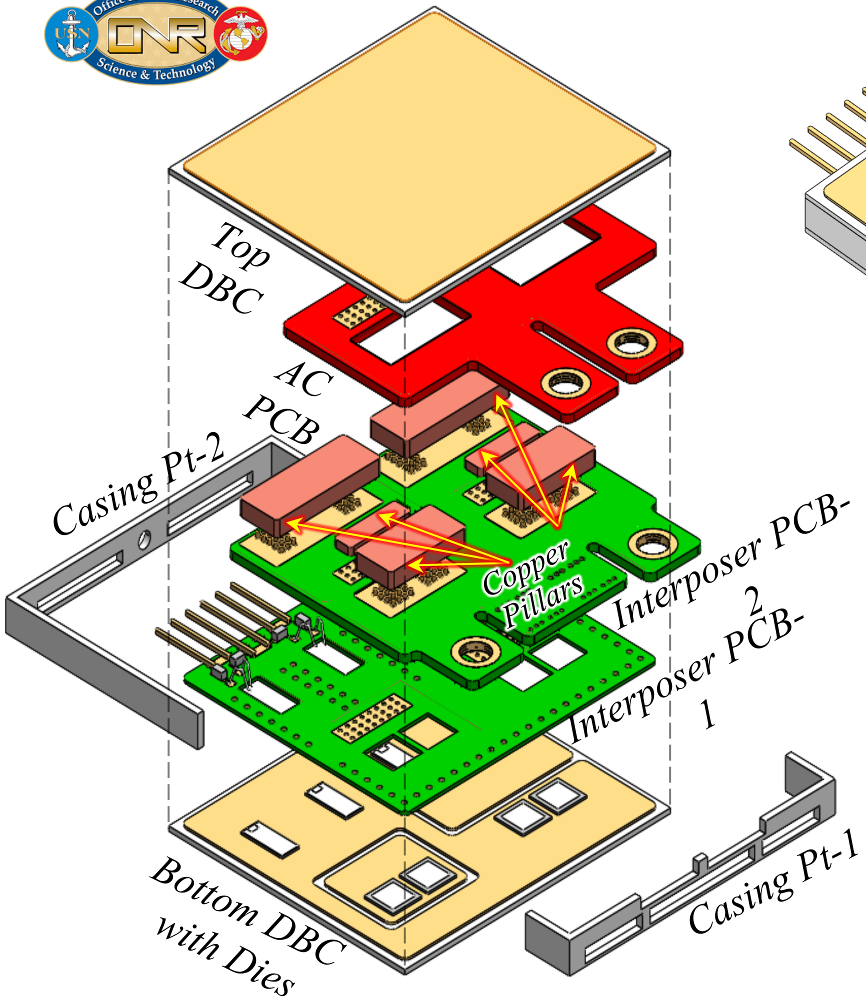
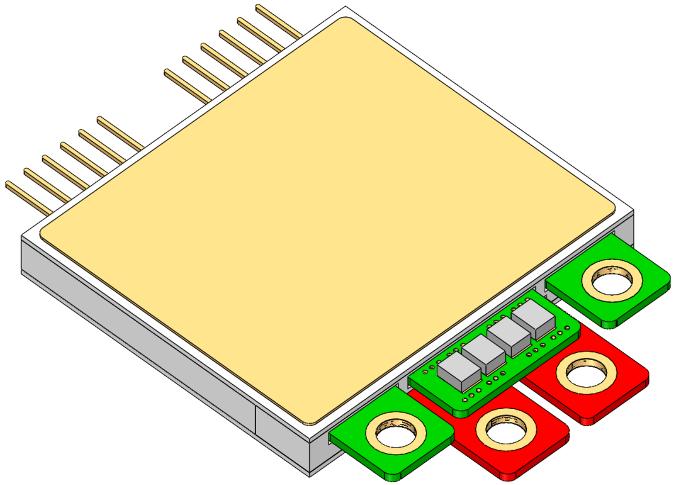
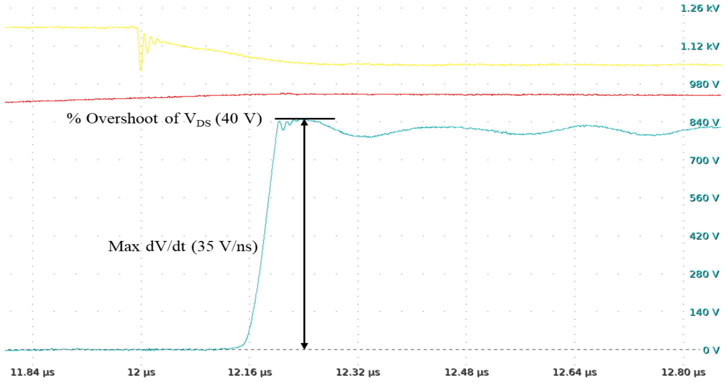
Solder-less 3D Integrated 1.2 kV/200A SiC Module

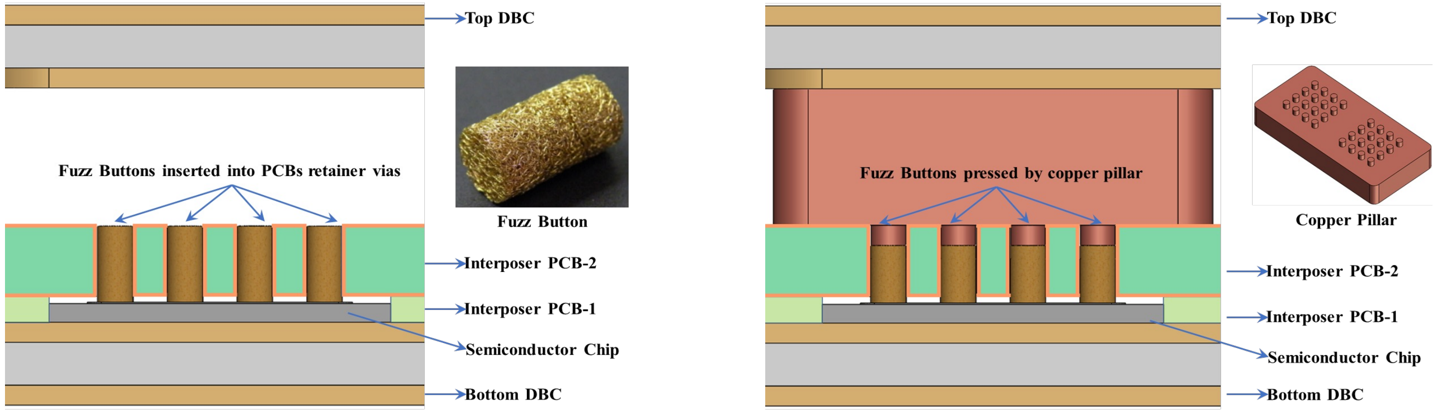


Exploded View



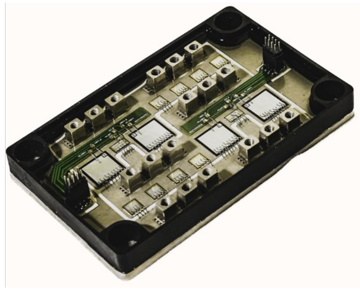


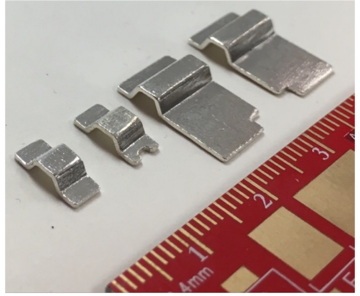
Turn off waveform (5% Overshoot, 800V/150A)

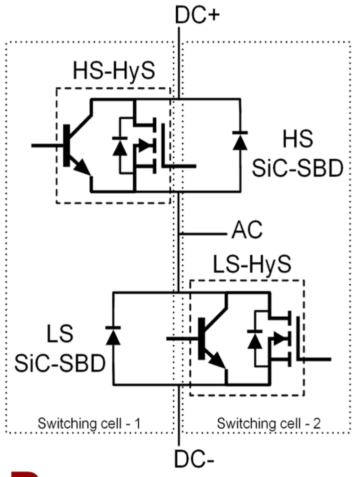


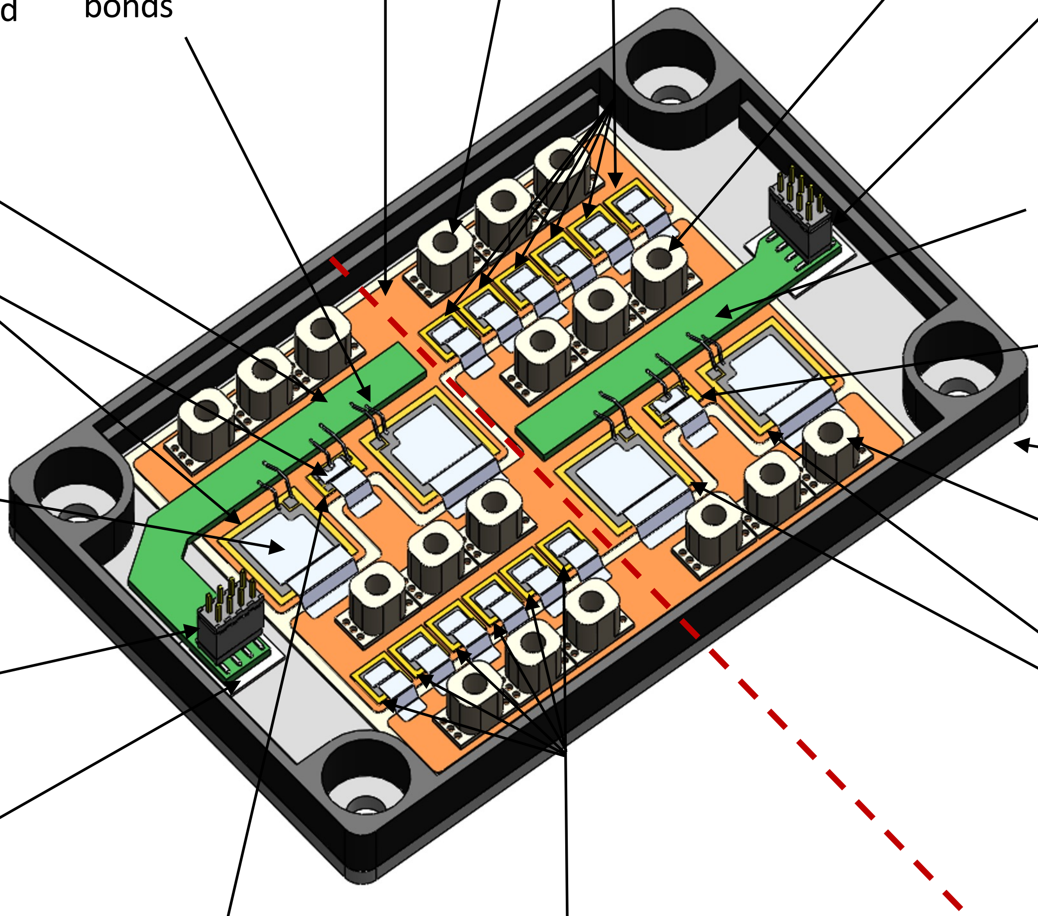
Use of Fuzz Button to establish pressure contact from the topside of the die

Si IGBT + SiC MOSFET Hybrid Switch Module

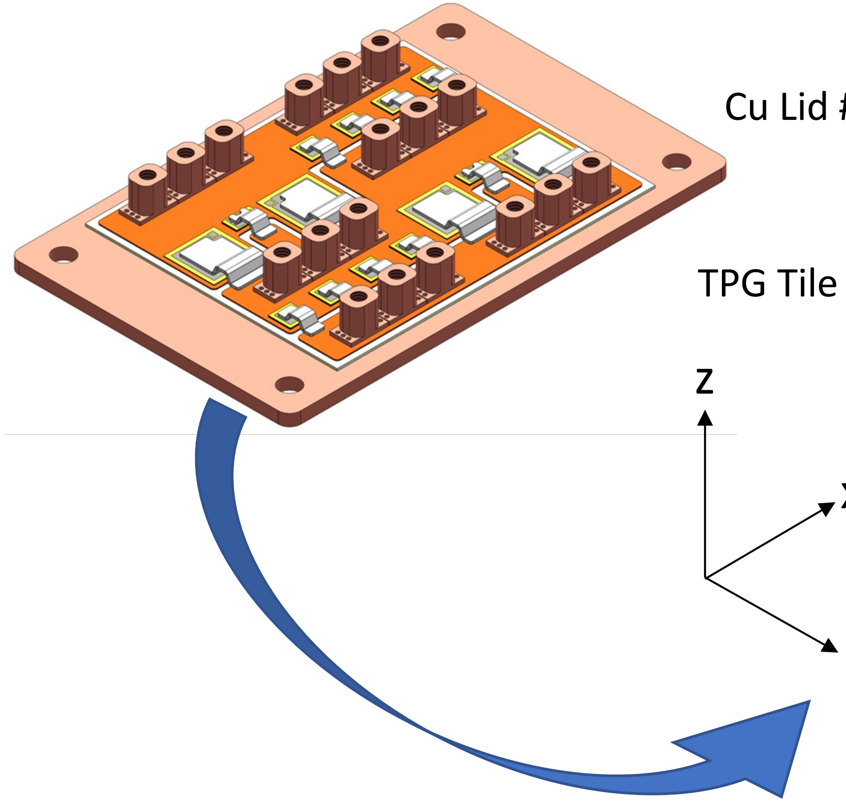


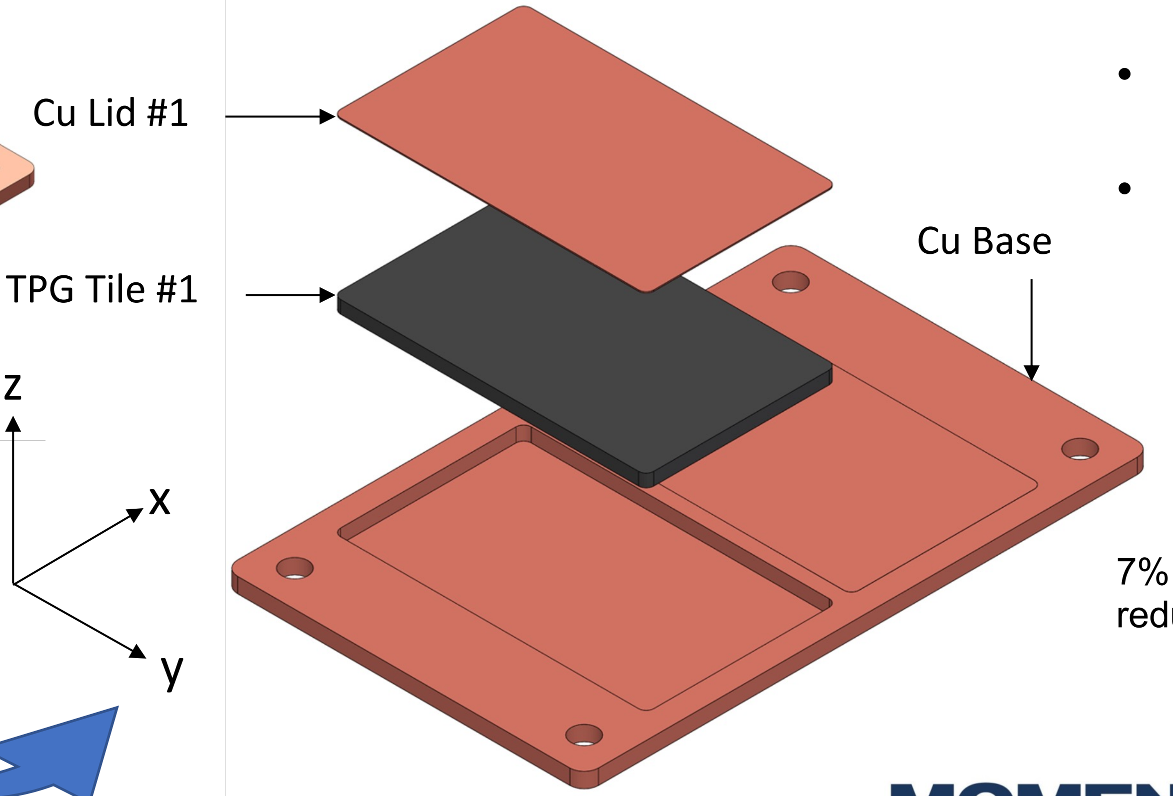






Metal encapsulated TPG Baseplate



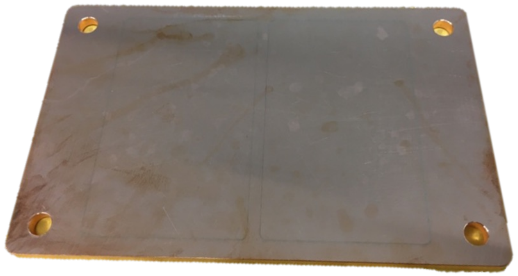


- Enhanced heat-removal
- Reduced thermal coupling between Si and SiC devices

7% temperature reduction is observed

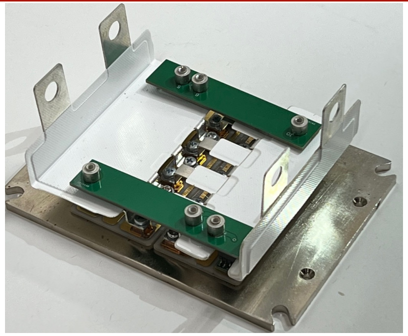
Elements	Qty	k_x (W/mK)	k_y (W/mK)	k_z (W/mK)
Cu Lid	2	400		
TPG Tile	2	10	1500	1500
Cu Base	1	400		

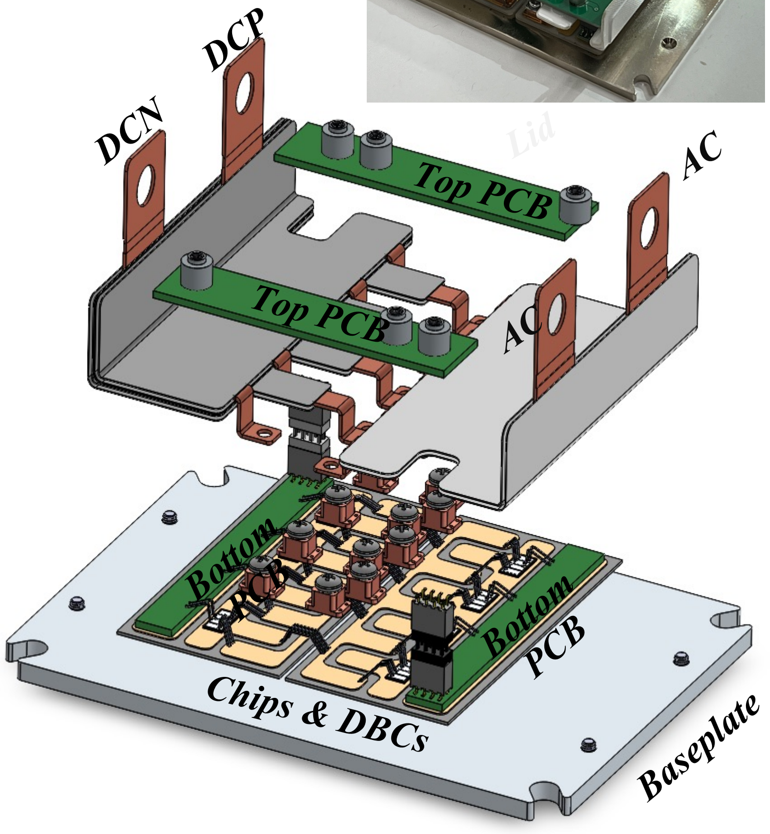
MOMENTIVE™



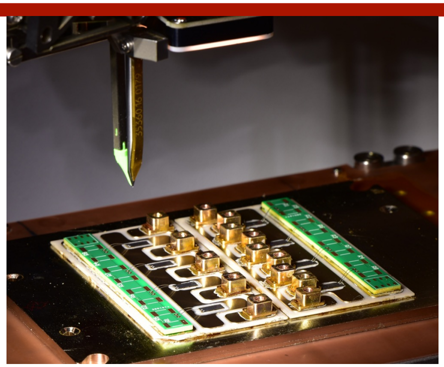
Custom Sample

3.3 kV SiC Phase-leg Module

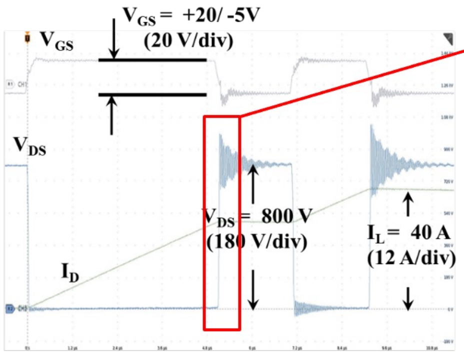




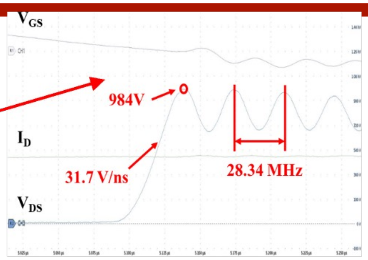
Exploded view *(Housing is removed)*



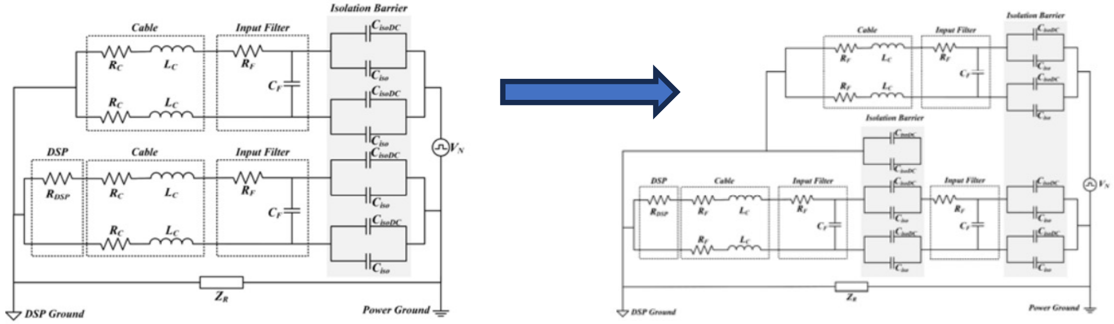
Balanced Layout for current sharing



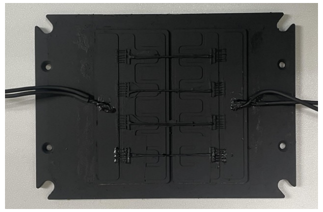
Switching waveform



Turn off transient



Cascaded Noise Hardened Gate Driving



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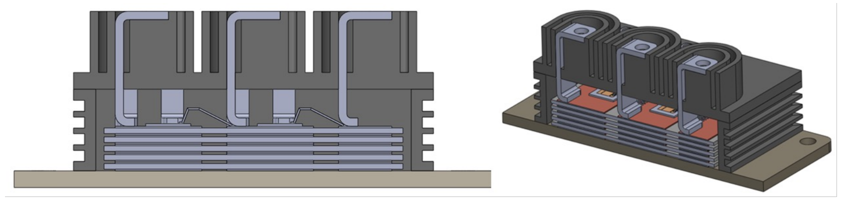
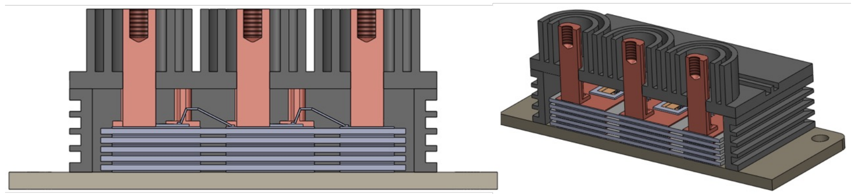
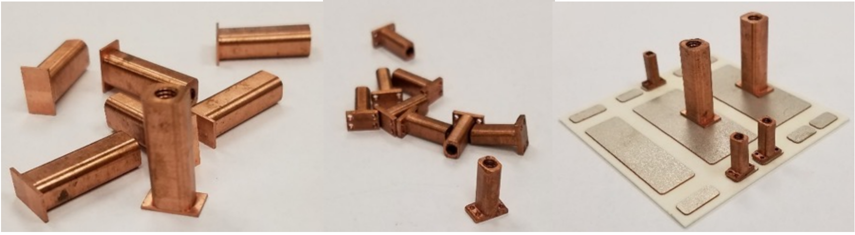
Stack-DBC 15kV SiC Module

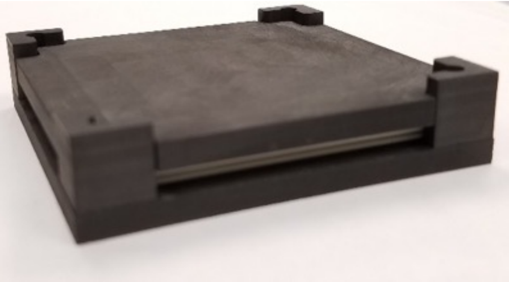


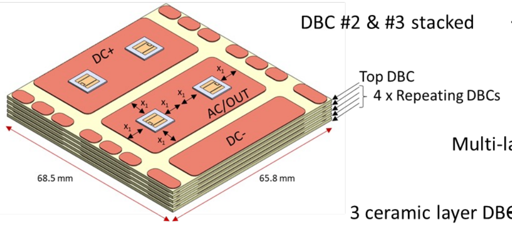
Module Cross-sections with busbar-like power terminals

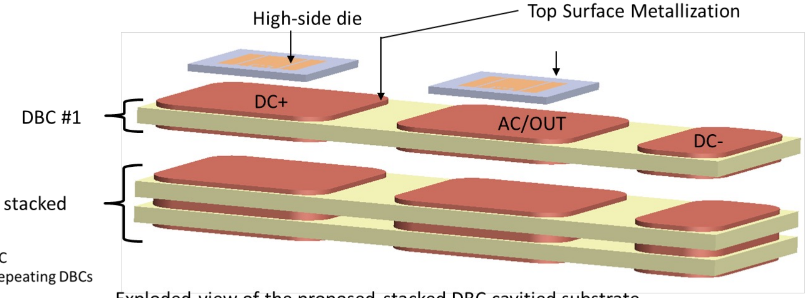


Module Cross-sections with power terminal blocks

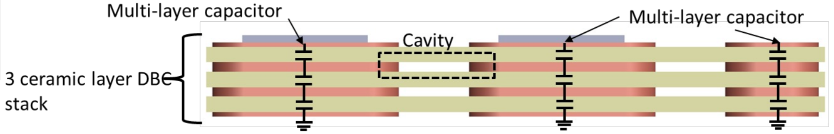








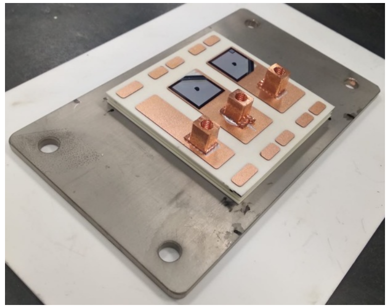
Exploded view of the proposed stacked DBC cavitied substrate

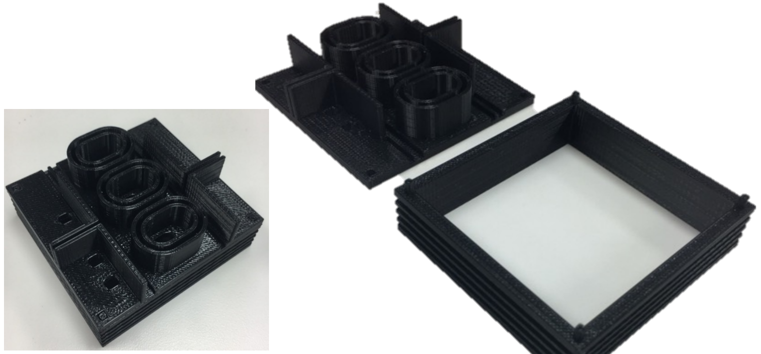


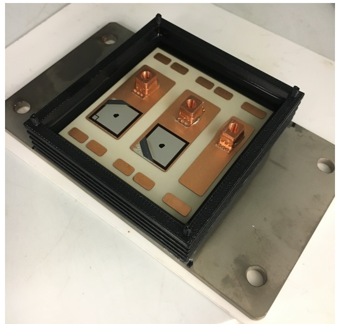
Cross-section view of the proposed solution showing resultant cavities

Housing Materials

1. ABS
   - Dielectric Strength: 15-34 kV/mm [1]
   - CTI Group: II
2. PTFE
   - Dielectric Strength: 17-24 kV/mm [1]
   - CTI Group: I







FAR BEYOND

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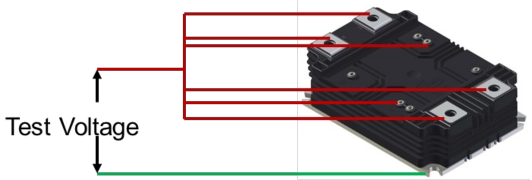
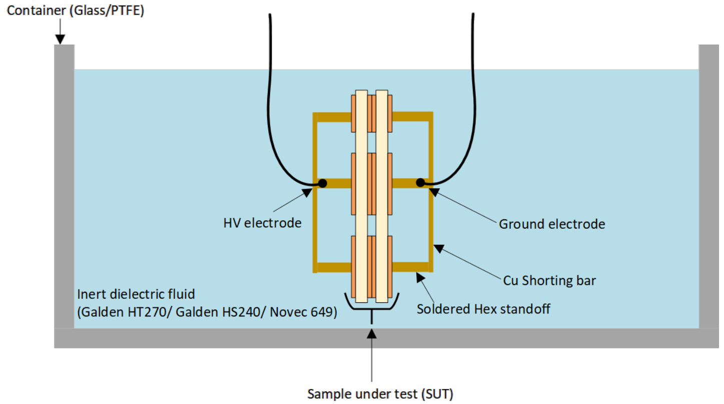
Insulation Testing

- Mandated by IEC 61287-1 (superseded IEC 1287)

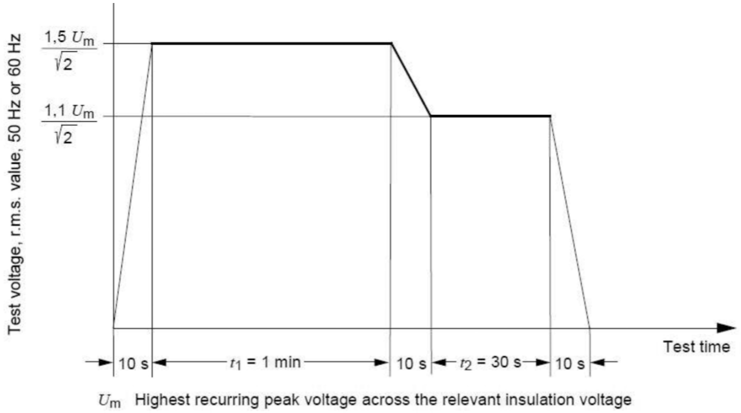
U_m = Blocking voltage of the module
60 s insulation test:
U_m = Blocking voltage of the module
Pass:
Component: 10 pC
Subassembly: 50 pC
Limitations: Only tests the baseplate isolation

$$U_{p_{rms}} = \frac{2U_m}{\sqrt{2}} + 1000\ \mathrm{V}$$





Module Blocking Voltage (kV)	Test Voltage (kV_{rms}) @ 50 Hz
3.3	5.67
6.5	10.2
10	15.1
15	22.2



PCB Under DC Excitation at Different Pressure

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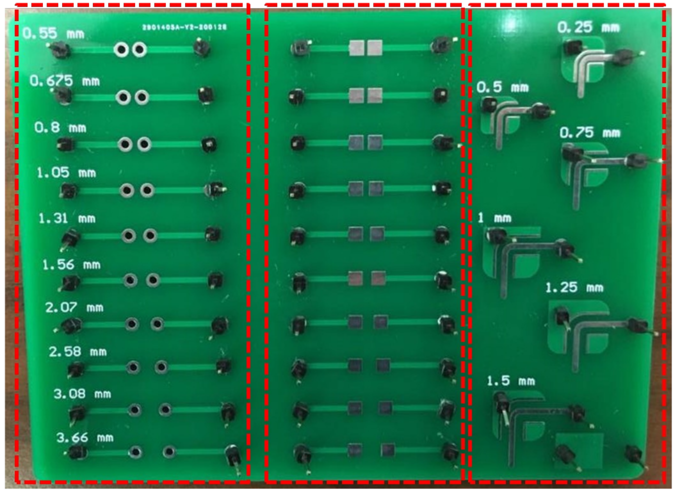
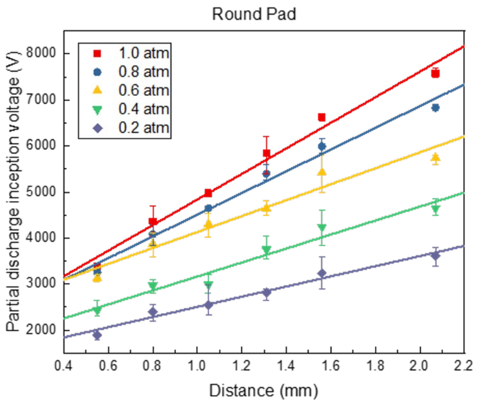
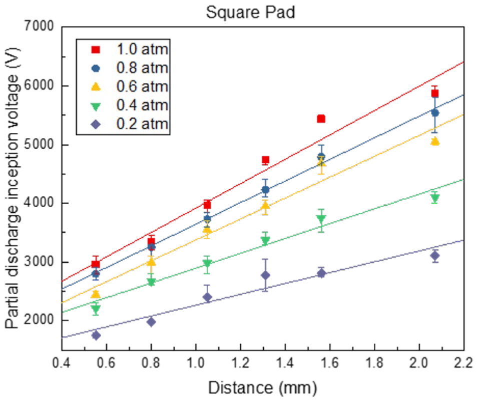


✓ *Round Pad* ✓ *Square Pad* ✓ *Trace Corner*

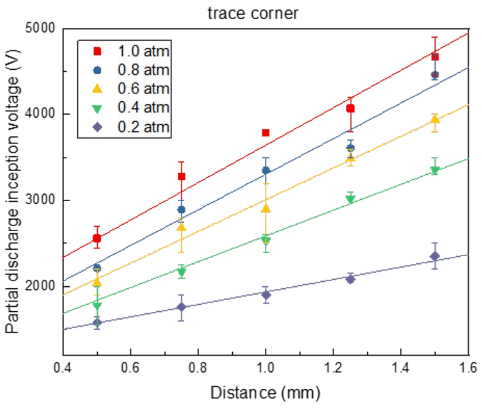
✓ *Round Pad*



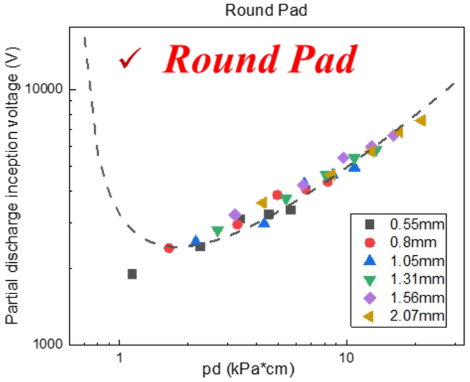
✓ *Square Pad*

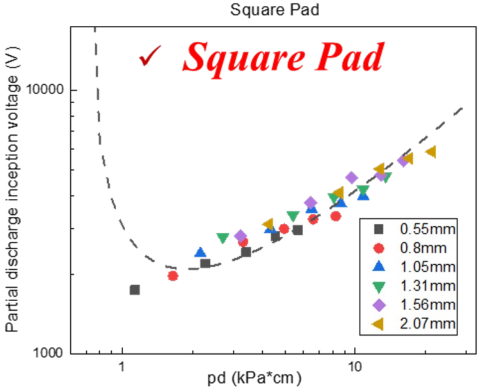


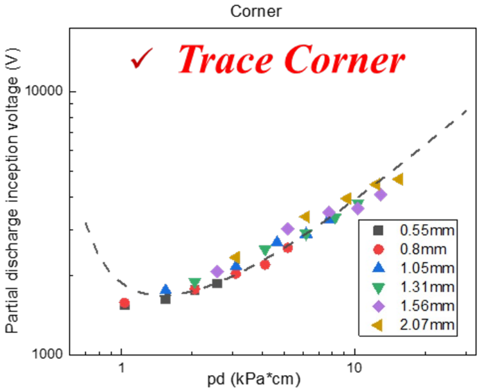
✓ *Trace Corner*



- Maximum creepage is ~2 mm
- PDIV: round pad > square pad > trace corner
- PDIV linearly increases with creepage at the same pressure
- The creepage range is not wide enough to see the saturation phenomenon, but the PDIV of round pad with 2 mm creepage is ~7500 V under DC voltage

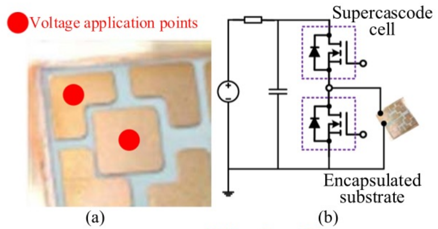


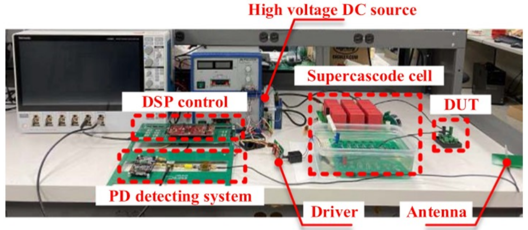


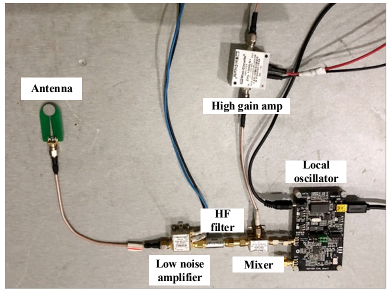


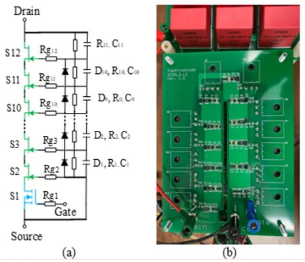
$$V_b = \frac{Bpd}{\ln Apd - \ln\left[\ln\left(1 + 1/\gamma_{se}\right)\right]}$$

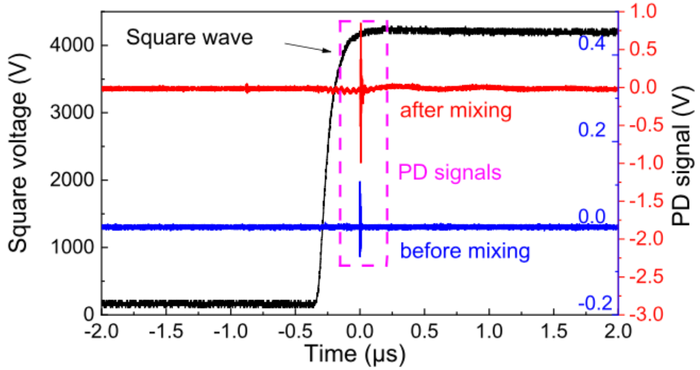
HV PWM Waveform Testing on Power Module

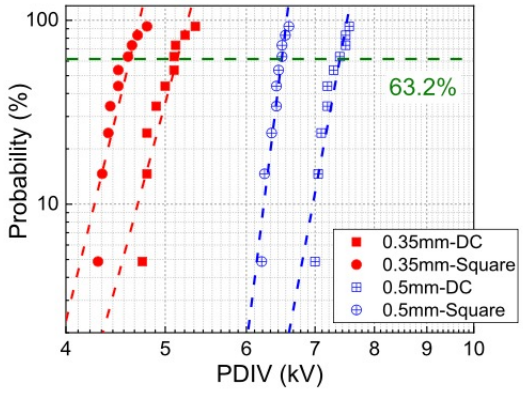


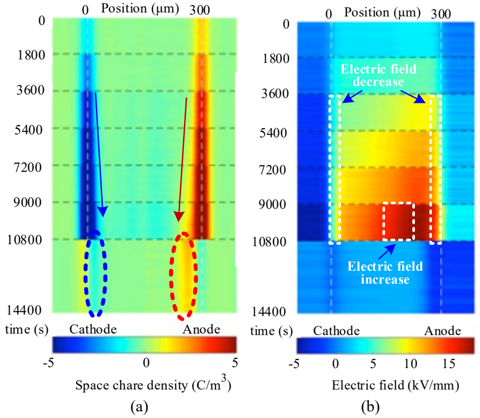






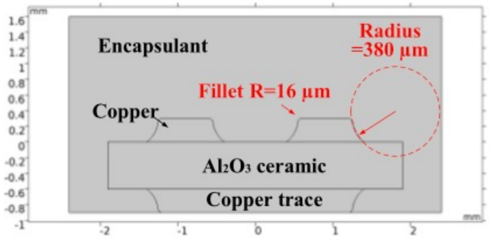


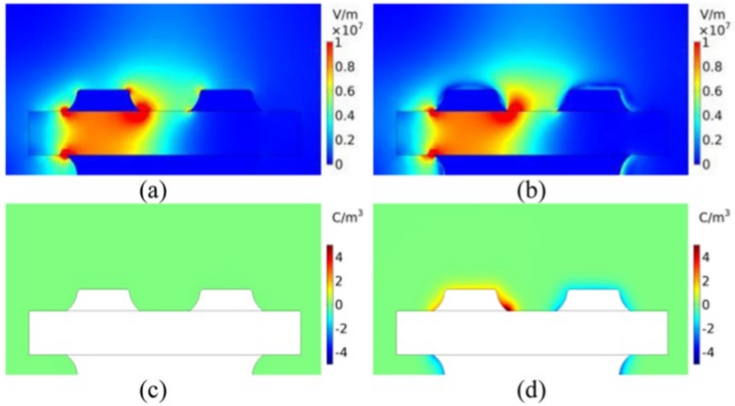




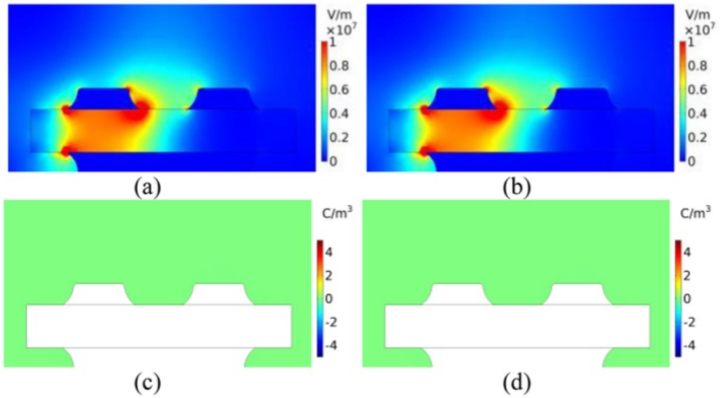
Space Charge

E-field





Space-charge simulation results under dc voltage. (a) Electric field distribution at 1 s. (b) Electric field distribution at 1800 s. (c) Space-charge distribution at 1 s. (d) Space-charge distribution at 1800 s.



Space-charge simulation results under dc voltage. (a) Electric field distribution at 1 s. (b) Electric field distribution at 1800 s. (c) Space-charge distribution at 1 s. (d) Space-charge distribution at 1800 s.

- PWM wave will influence space charge distribution in insulator
- Change of space charge will influence E-field distribution

Conclusion and Discussion

- Co-design and co-optimization efforts are required to achieve overall module performance balancing
- Layout optimization is needed for both thermal decoupling as well as switching performance improvement
- EM design and noise mitigation control is critical for HV module design, module parasitics can be used for dV/dt control.
- E-field grading and active dV/dt control are also important while worth more effort