Power Electronics & Energy Conversion Workshop, Sandia National Labs

Reliability Characterization and In-Situ Health Estimation of WBG Semiconductor-Based Power Converters

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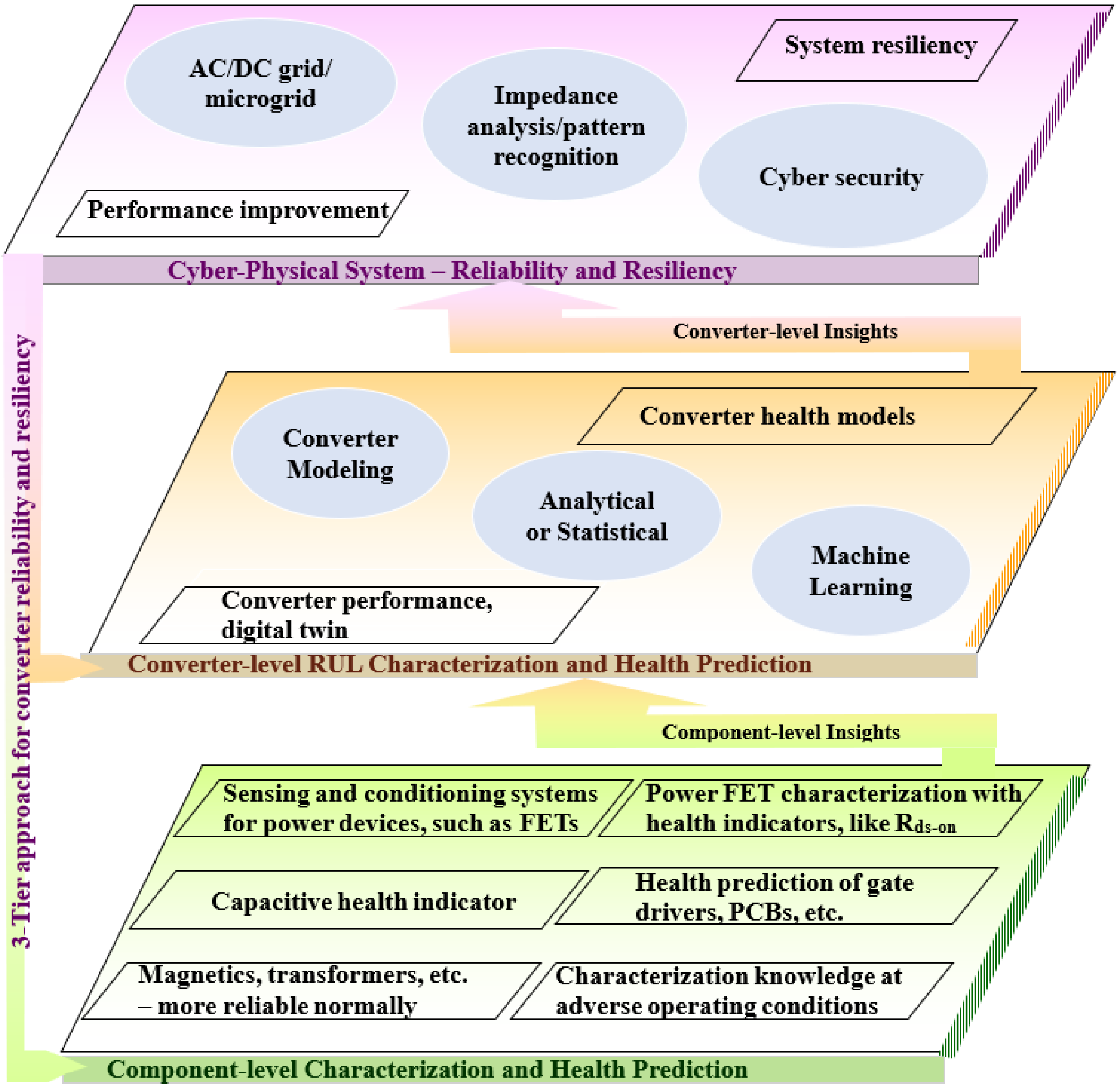
Harish S. Krishnamoorthy, Ph.D.
Assistant Professor, ECE Department;
Associate Director, PEMSEC Consortium

Sandia National Laboratories

UNIVERSITY of
HOUSTON
CULLEN COLLEGE of ENGINEERING

3-Tier Approach for Resiliency and Health

- Component-level characterization and prediction of remaining useful lifetime (RUL)
- Converter or sub-system level health assessment
- Cyber-physical system (CPS) reliability and resiliency



AC/DC grid/ microgrid

Impedance analysis/pattern recognition

System resiliency

Cyber security

Performance improvement

Cyber-Physical System – Reliability and Resiliency

Converter-level Insights

Converter Modeling

Converter health models

Analytical or Statistical

Machine Learning

Converter performance, digital twin

Converter-level RUL Characterization and Health Prediction

Component-level Insights

Sensing and conditioning systems for power devices, such as FETs

Power FET characterization with health indicators, like $R_{ds\text{-}on}$

Capacitive health indicator

Health prediction of gate drivers, PCBs, etc.

Magnetics, transformers, etc. – more reliable normally

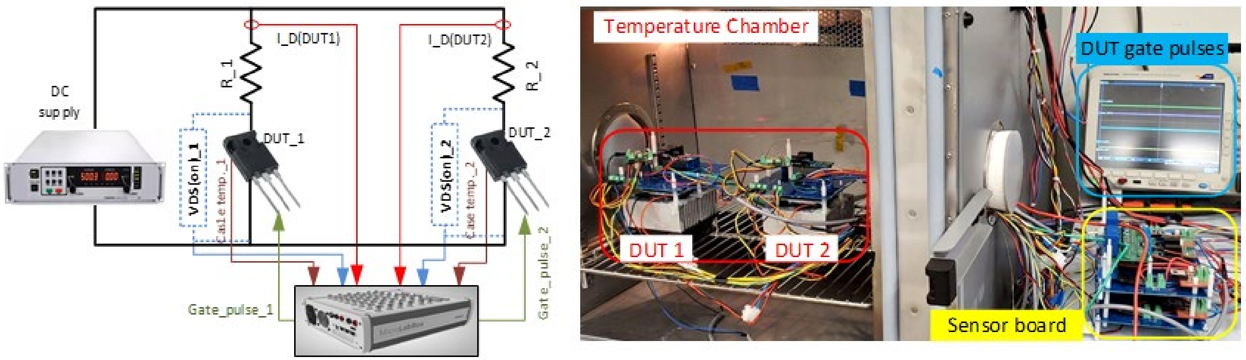
Characterization knowledge at adverse operating conditions

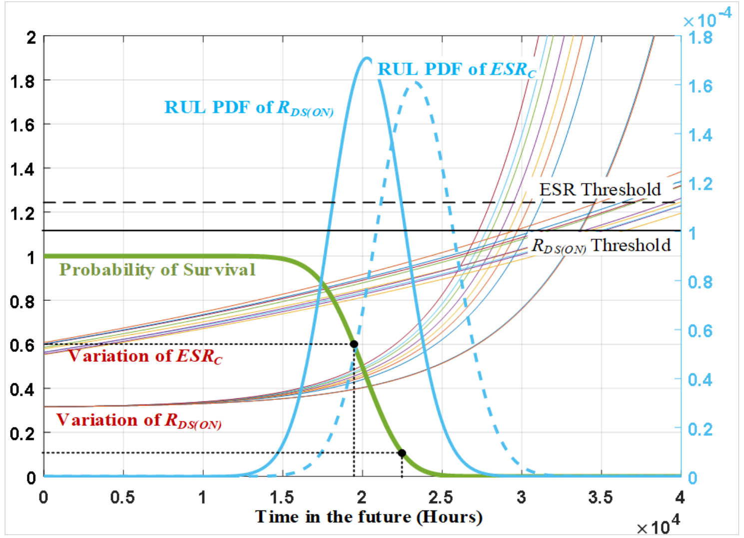
Component-level Characterization and Health Prediction

3-Tier approach for converter reliability and resiliency

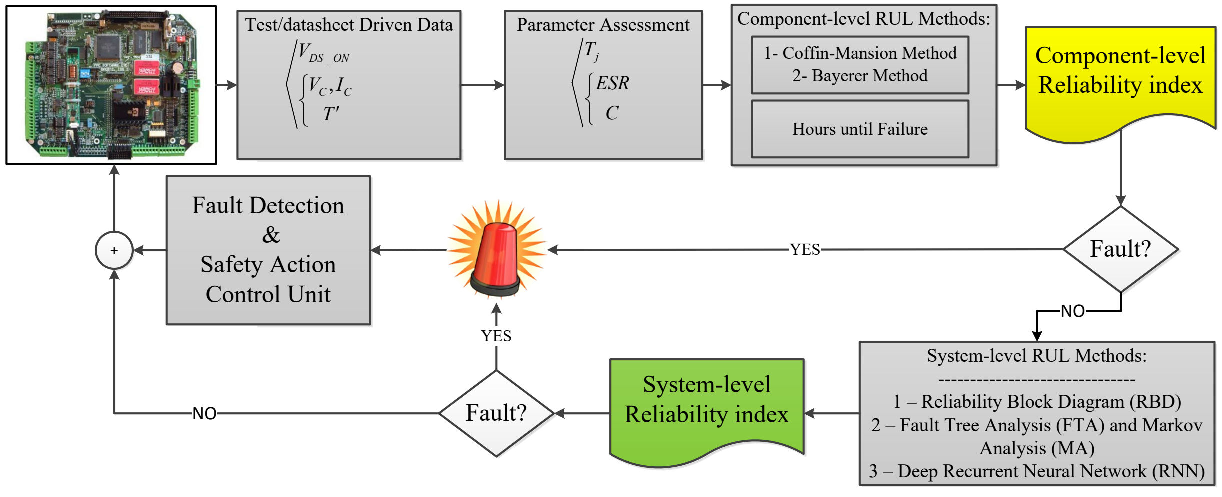
Device Characterization Approach

Test setup for device degradation





RUL PDFs and Probability distribution of converter survival



Test/datasheet Driven Data

V_{DS_ON}, V_C, I_C, T'

Parameter Assessment

T_j, ESR, C

Component-level RUL Methods:

1- Coffin-Mansion Method
2- Bayerer Method

Hours until Failure

Component-level Reliability index

Fault?

YES

NO

Fault Detection & Safety Action Control Unit

System-level RUL Methods:

1 – Reliability Block Diagram (RBD)
2 – Fault Tree Analysis (FTA) and Markov Analysis (MA)
3 – Deep Recurrent Neural Network (RNN)

System-level Reliability index

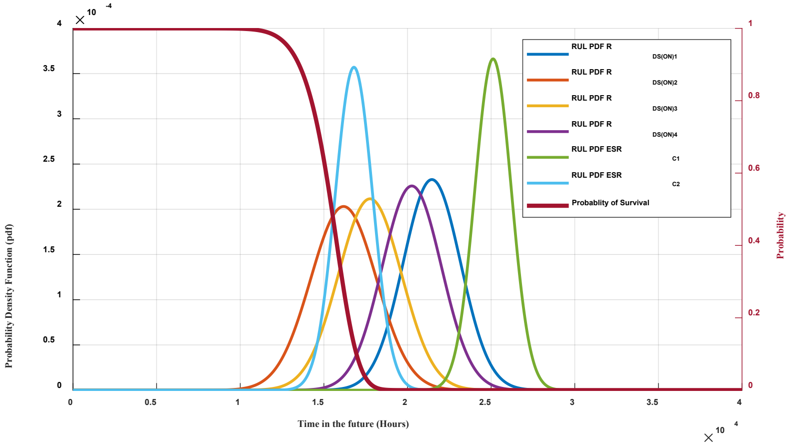
Fault?

YES

NO

+

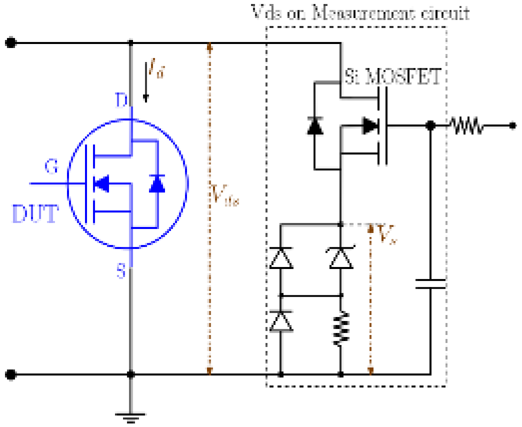
System-level RUL prediction flowchart



A. Sadat and H. S. **Krishnamoorthy**, "Measure Theory-based Approach for Remaining Useful Lifetime Prediction in Power Converters," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA

FET – based $R_{DS\text{-}on}$ Measurement

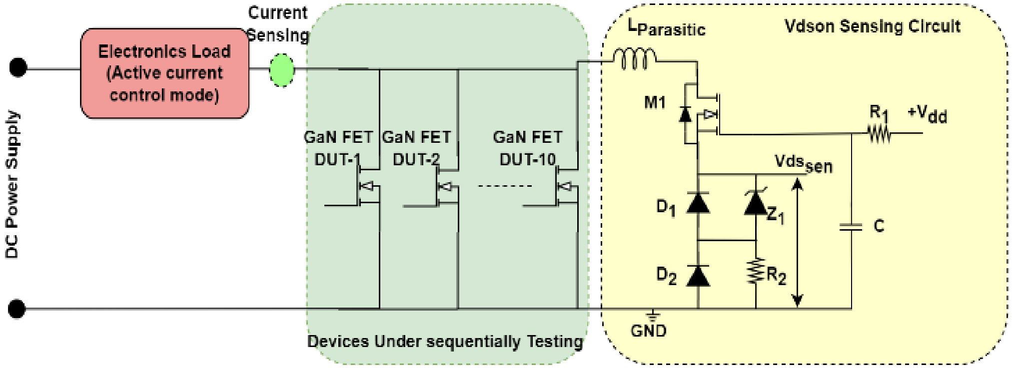
- This Rds-on measurement circuit uses a FET, two Schottky diodes, and a Zener diode (with a resistor).
- Gate voltage is greater than the threshold voltage; almost equal to the Zener diode voltage is always applied on the auxiliary FET
- When the DUT is off, the Gate source voltage of the aux. FET is less than the Gate threshold voltage; hence, it is off, blocking the DUT's off voltage. The sensed voltage Vs will be just the Zener diode voltage.
- When the DUT turns on, the Gate source voltage of the aux. FET will be greater than the Gate threshold voltage hence the aux. FET will be turned on. The voltage across the aux. FET will be less than mV range; hence, the Vs directly measures the $V_{ds\text{-}on}$

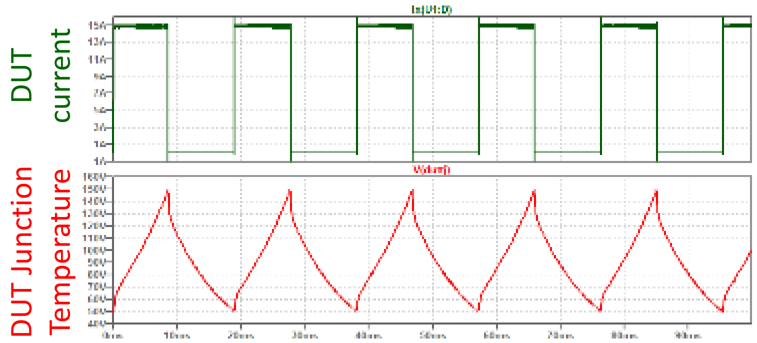


FET-based Rds-on measurement circuit (referred by JEDEC JEP173 guidelines)

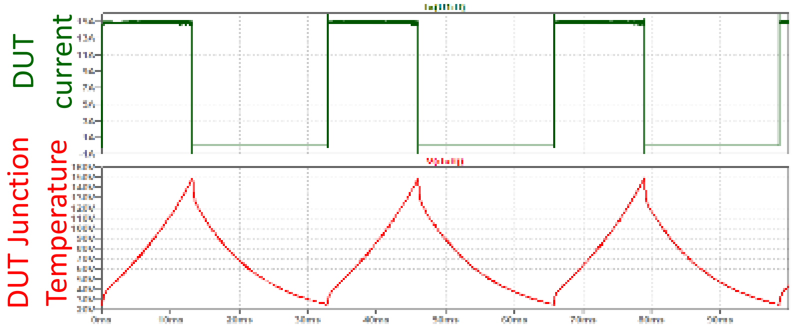
Degradation Profile – Thermal Cycling

- Set-up contains 3 stages: current source, DUT, and Rds-on measurement.
- To degrade multiple GaN devices together, they are connected in parallel.
- A constant current stress has been simulated using LTSpice software and from the figures, it could be observed the GaN device gets heated up and cooled down with current stress.

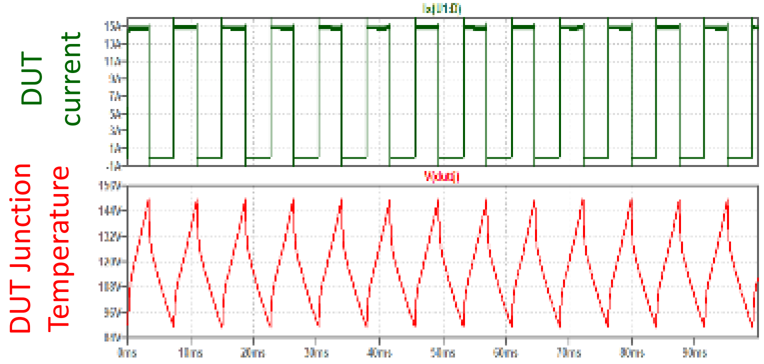




Temperature cycling between 50^0C to 150^0C



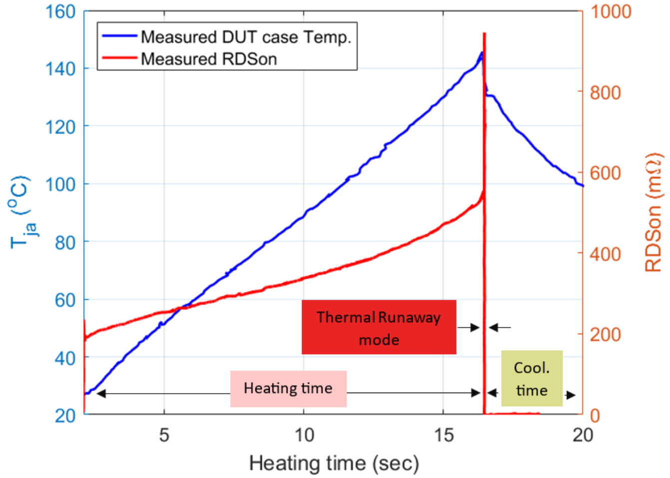
Temperature cycling between 25^0C to 150^0C

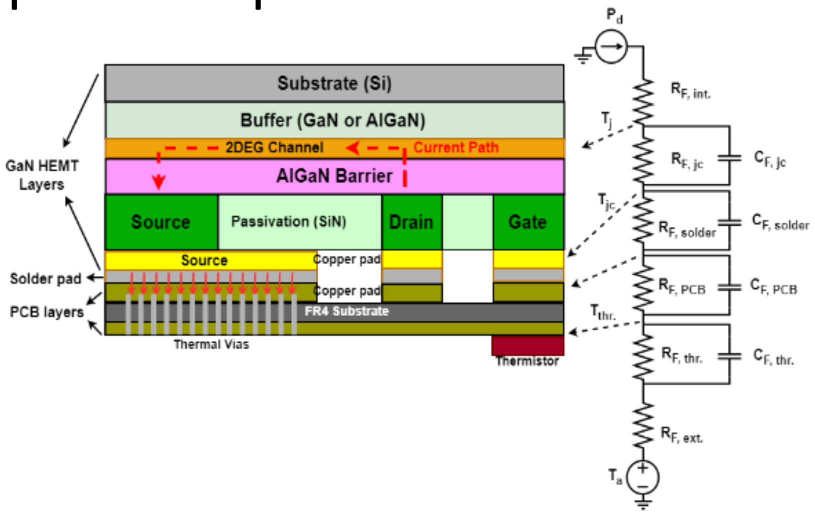


Temperature cycling between 90^0C to 150^0C

Performing Thermal Cycling with GaN FETs

- Measured the temperature on-board using a thermistor, initially
- The current was kept constant, but, power dissipation was not constant due to the on-state resistance change
- The time constant from the device channel to the thermistor caused a significant delay in the measurement
- Thermal runaway was observed, so had to formulate a different means to detect the peak temperature





Modeling the Time Constant

$$Z_{ja} = Z_{F1} + Z_{F2} + Z_{F3} + \cdots + Z_{Fn} \qquad T_j(t) = P_d(t).Z_{ja} + T_a$$

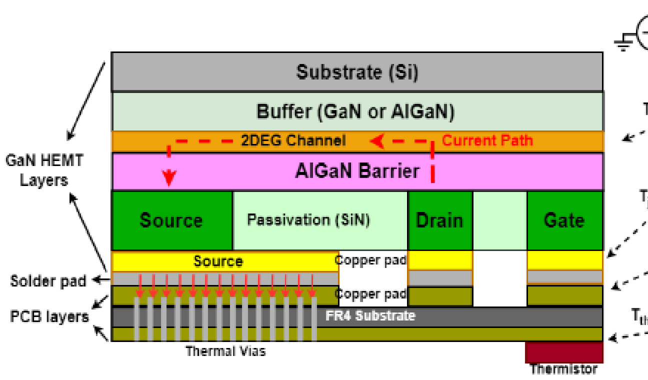
$$Z_{ja}(s) = \frac{R_{F1}}{\tau_1 s + 1} + \frac{R_{F2}}{\tau_2 s + 1} + \frac{R_{F3}}{\tau_3 s + 1} + \cdots + \frac{R_{Fn}}{\tau_n s + 1}$$

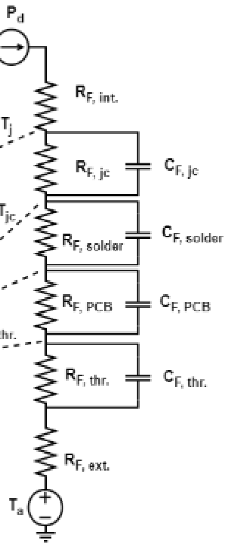
$$Z_{thr}(t) = \frac{T_{thr}(t) - T_a}{P_d(t)} \qquad \boxed{Z_{thr}(t) = a\ .\ e^{-b.t} + c}$$

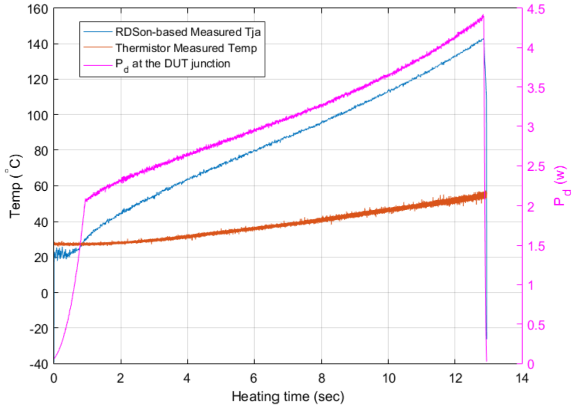
$$\frac{R_{F,thr}}{\tau_{thr}} e^{-\frac{t}{\tau_{thr}}} + R_{ext} = 1.23 * \ e^{-0.25*t} + 12.4$$

$$Z_{j-thr}(t) = \frac{T_{Tj-RDSon}(t) - T_{thr}(t)}{P_d(t)} \qquad \boxed{Z_{j-thr}(t) = a\ .\ e^{-b.t} + c\ .\ e^{-d.t} + g}$$

$$\frac{R_{F,jc}}{\tau_{jc}} e^{-\frac{t}{\tau_{jc}}} + \frac{R_{F,PCB-solder}}{\tau_{PCB-solder}} e^{-\frac{t}{\tau_{PCB-solder}}} + R_{int} = 5.662 * \ e^{-4.t} + 288.8 * \ e^{-8.t} + 22.6$$

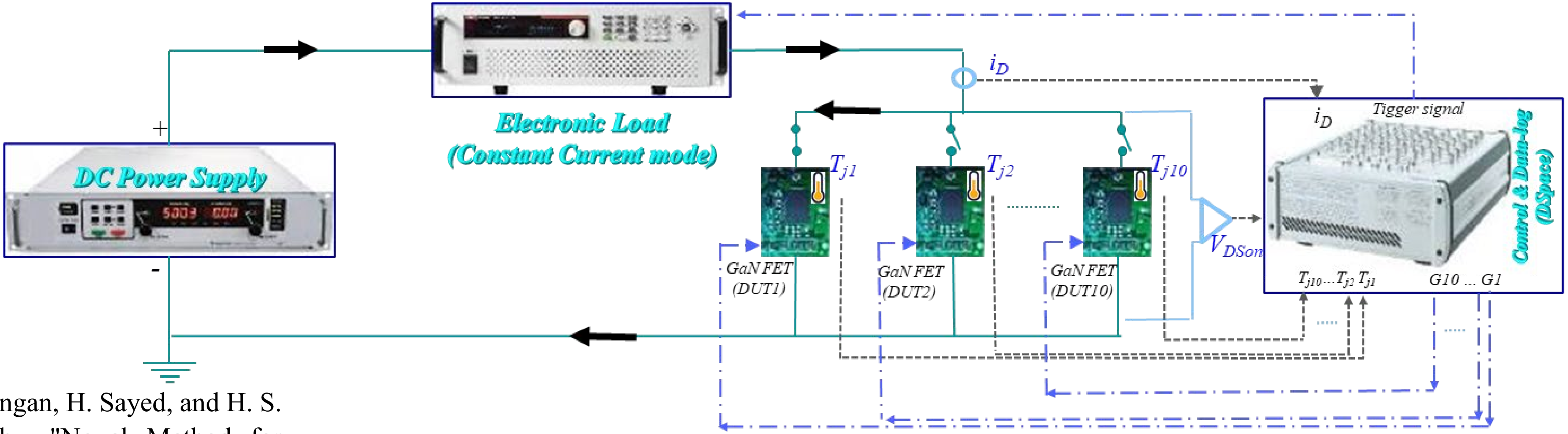




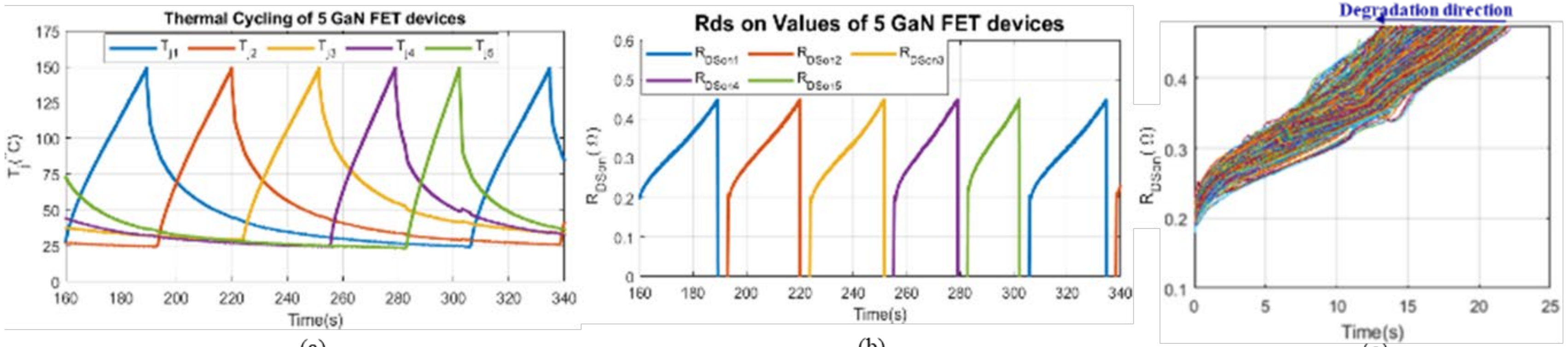


Components	Thermal time constant	Thermal impedance
GaN HEMT	250 ms	$R_{F,jc}$=1.4155 °C/W $C_{F,jc}$= 177 mJ/°C
PCB layout, including 20 vias underneath DUT and solder joints	125 ms	$R_{F,PCB-solder}$=36.1 °C/W $C_{F,PCB-solder}$= 3.463 mJ/°C R_{int}=22.6 °C/W
Thermistor	4 s	$R_{F,thr}$=4.92 °C/W $C_{F,thr}$= 813 mJ/°C R_{ext}=12.4 °C/W

GaN Degradation Setup



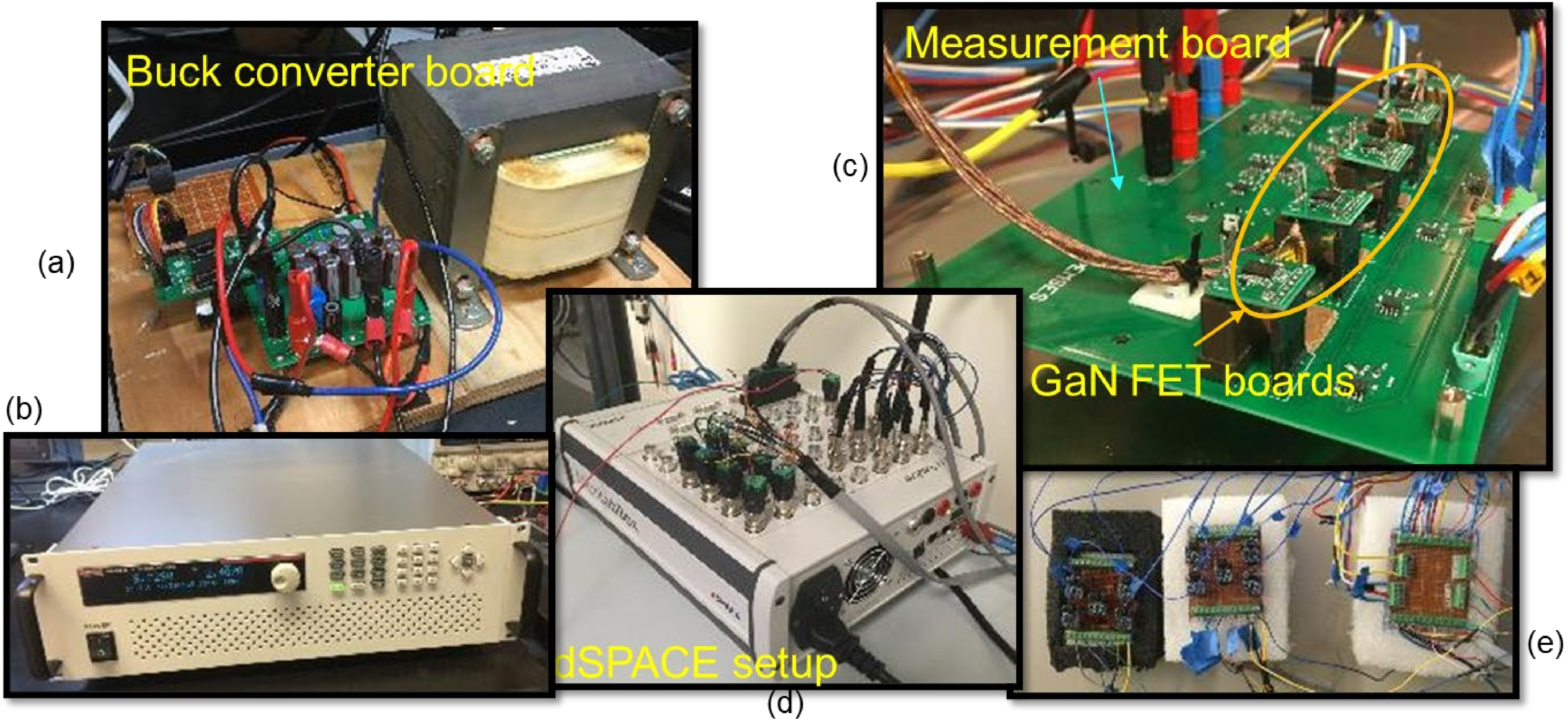
1. G. S. Kulothungan, H. Sayed, and H. S. Krishnamoorthy, "Novel Method for Accelerated Thermal Cycling of Gallium Nitride Power Devices to Perform Reliability Assessment", in the IEEE Applied Power Electronics Conference (APEC), Mar. 2022, Houston, TX, USA
2. H. Sayed, G. S. Kulothungan, H. S. Krishnamoorthy, "Dynamic Remaining Useful Lifetime (RUL) Estimation of Power Converters based on GaN Power FETs", in the IEEE Applied Power Electronics Conference (APEC), Mar. 2022, Houston, TX, USA



(a) (b) (c)

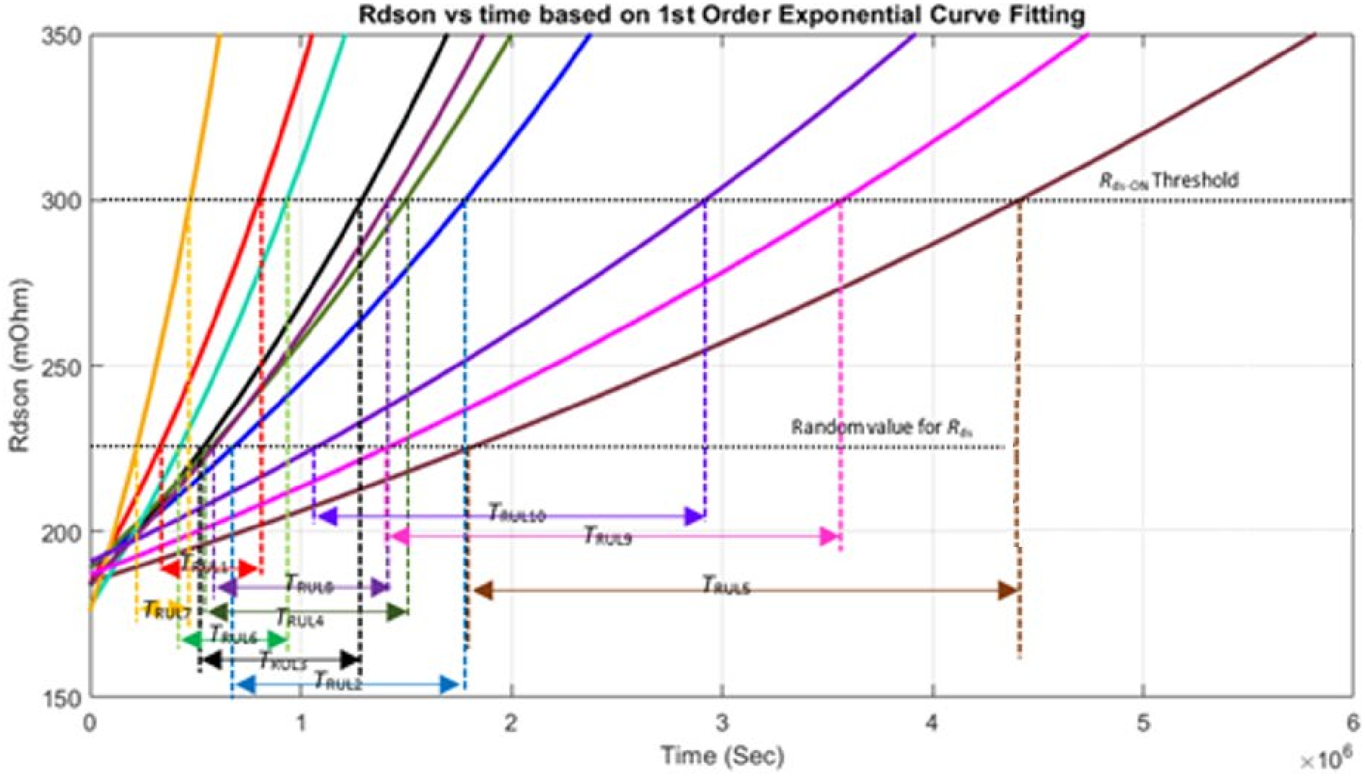
Fig. (a) Junction temperature & (b) Rds-on values captured during thermal cycling . (c) Variation of the Rds-on over many Thermal cycles

GaN Degradation Setup



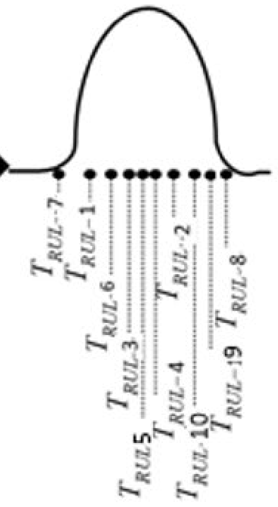
Test set-up with (a) the buck converter or (b) Electronic load for current control, (c) measurement board with the GaN FET boards, (d) dSPACE setup for control and data logging and (e) Thermocouple amplifiers

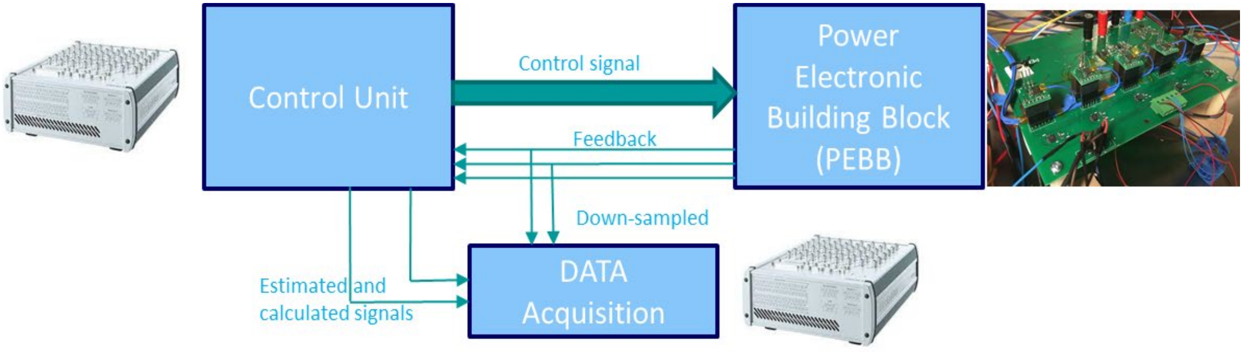
Measure Theory – based RUL Prediction



$T_{RUL1} = t_{EOL1} - t_1$
$T_{RUL2} = t_{EOL2} - t_2$
$T_{RUL3} = t_{EOL3} - t_3$
$T_{RUL4} = t_{EOL4} - t_4$
$T_{RUL5} = t_{EOL5} - t_5$
$T_{RUL6} = t_{EOL6} - t_6$
$T_{RUL7} = t_{EOL7} - t_7$
$T_{RUL8} = t_{EOL8} - t_8$
$T_{RUL9} = t_{EOL9} - t_9$
$T_{RUL10} = t_{EOL10} - t_{10}$

PDF of time distribution for calculated RUL





Control Unit

Control signal

Power Electronic Building Block (PEBB)

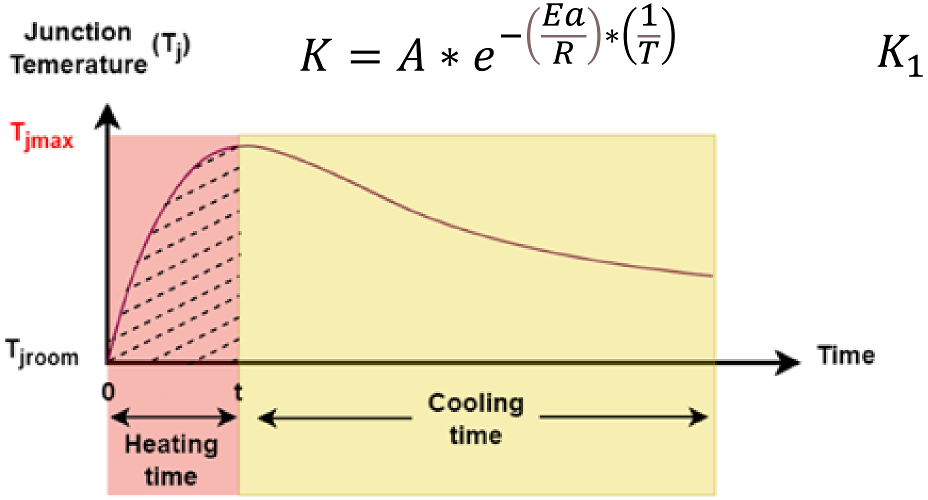
Feedback

Down-sampled

Estimated and calculated signals

DATA Acquisition

Extracting Component-level Activation Energy



$$K = A * e^{-\left(\frac{Ea}{R}\right)*\left(\frac{1}{T}\right)}$$

$$K_1 = A * e^{-\left(\frac{Ea}{R}\right)*\left(\frac{1}{T_1}\right)}$$

$$K_2 = A * e^{-\left(\frac{Ea}{R}\right)*\left(\frac{1}{T_2}\right)}$$

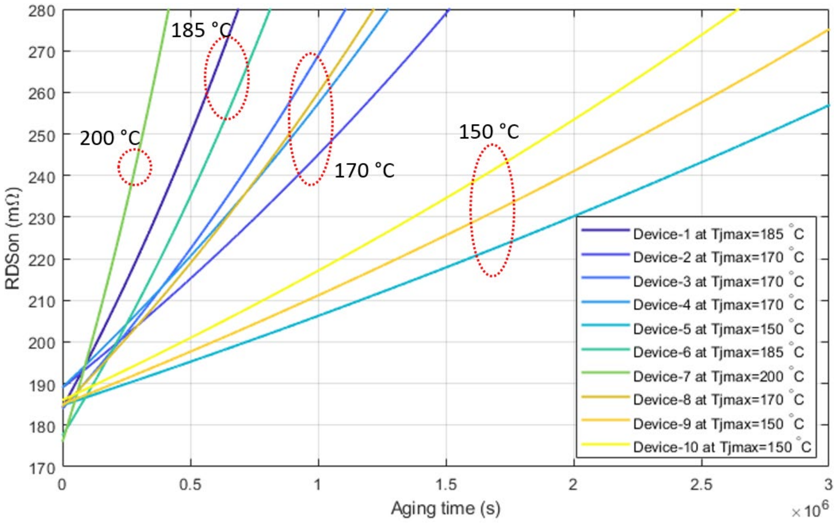
$$T_1 = \frac{1}{t_1} \cdot \int_0^{t_1} T_j(t)\, dt$$

$$\boxed{\boldsymbol{\frac{K_1}{K_2} = e^{-\left(\frac{Ea}{R}\right)*\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}}}$$

$$\frac{\ln\left(\frac{K_1}{K_2}\right)_{case\ 1}}{\ln\left(\frac{K_1}{K_2}\right)_{case\ 2}} \approx \frac{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)_{case\ 1}}{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)_{case\ 2}}$$

Case study	Thermal cycling window	Acceleration factor (k) = $\left(\frac{K_1}{K_2}\right)$	$\frac{1}{T}$ $(\mu K^{-1}) = \frac{1}{T_1 + 273} - \frac{1}{T_2 + 273}$
1	T_1 = 25-to-150 °C T_2 = 25-to-170 °C	$\frac{1.6}{0.6}$ = 2.67	$\frac{1}{360.5} - \frac{1}{370.5}$ = **74.87**
2	T_1 = 25-to-170 °C T_2 = 25-to-185 °C	$\frac{0.6}{0.3}$ = 2.00	$\frac{1}{370.5} - \frac{1}{378}$ = **53.55**

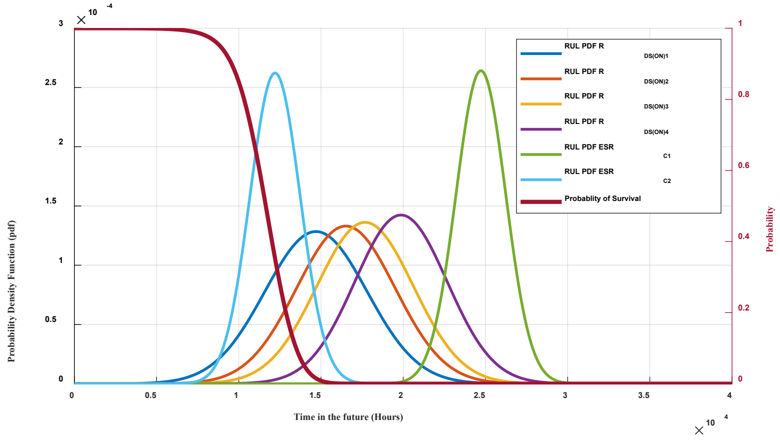
$$\frac{\ln(2.67)}{\ln(2.00)} = \frac{0.982}{0.693} \approx \frac{74.87\mu}{53.55\mu} \approx 1.4$$

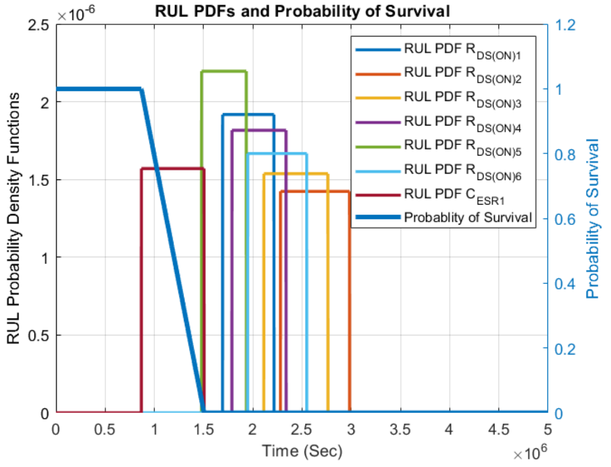


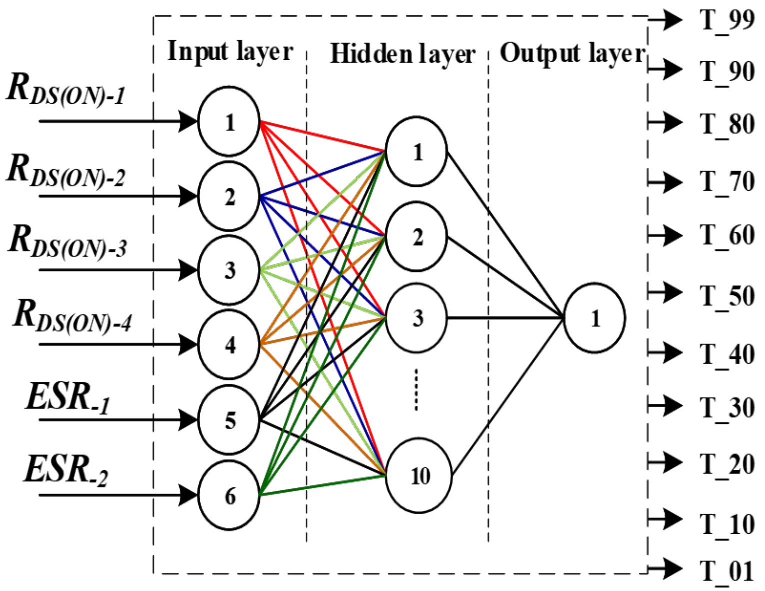
- The ratio of the acceleration factors (K) and the temperature terms of both cases is roughly equal to **1.4**.
- The Activation Energy (***E_a***) is ~***1.13*** *eV*

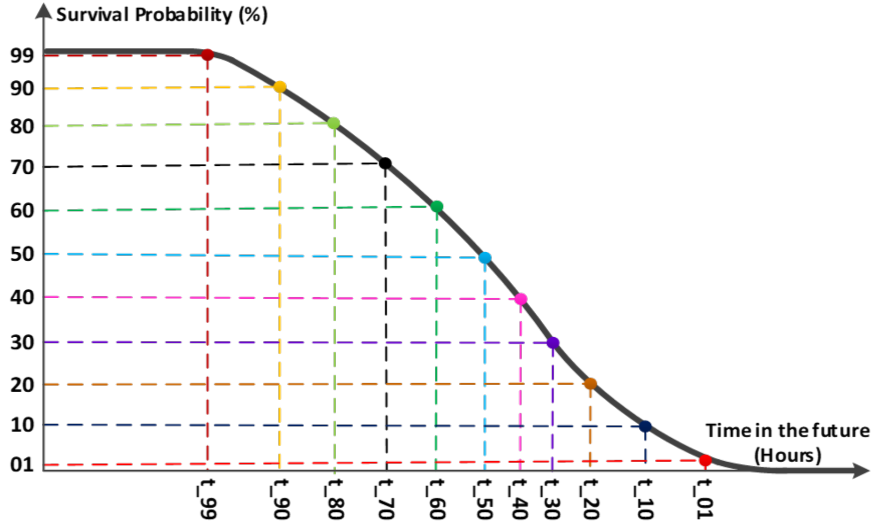
Source: H. Sayed, G. S. Kulothungan and H. S. Krishnamoorthy, "Characterization of GaN HEMTs' Aging Precursors and Activation Energy Under a Wide Range of Thermal Cycling Tests," in IEEE Open Journal of the Industrial Electronics Society, vol. 4, pp. 123-134, 2023, doi: 10.1109/OJIES.2023.3267004.

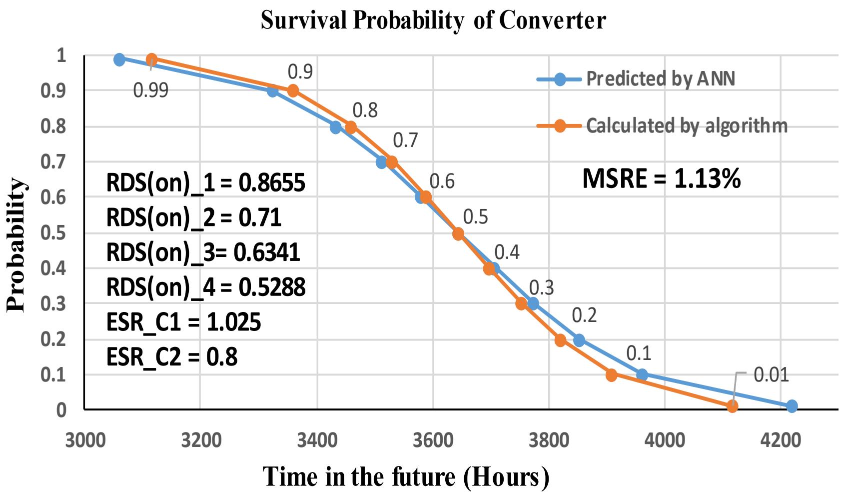
Machine Learning for In-situ Implementation





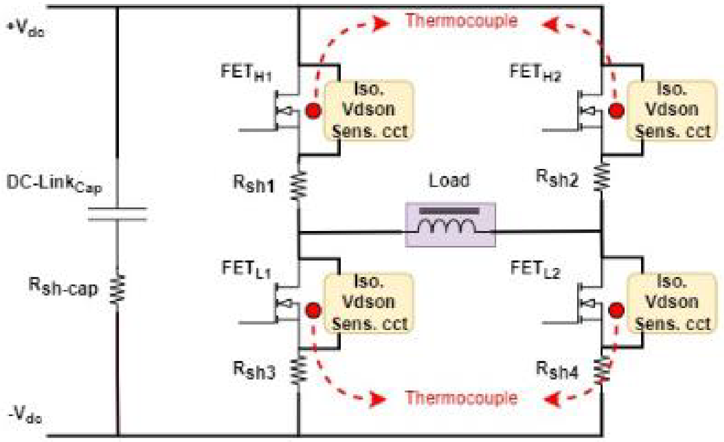


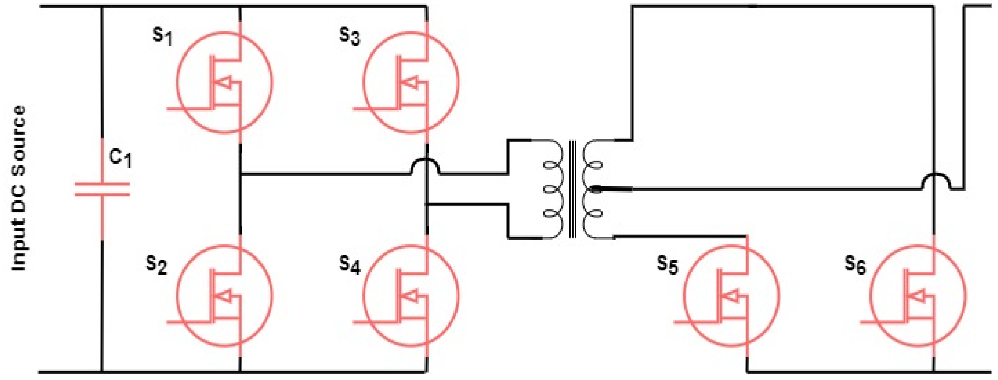


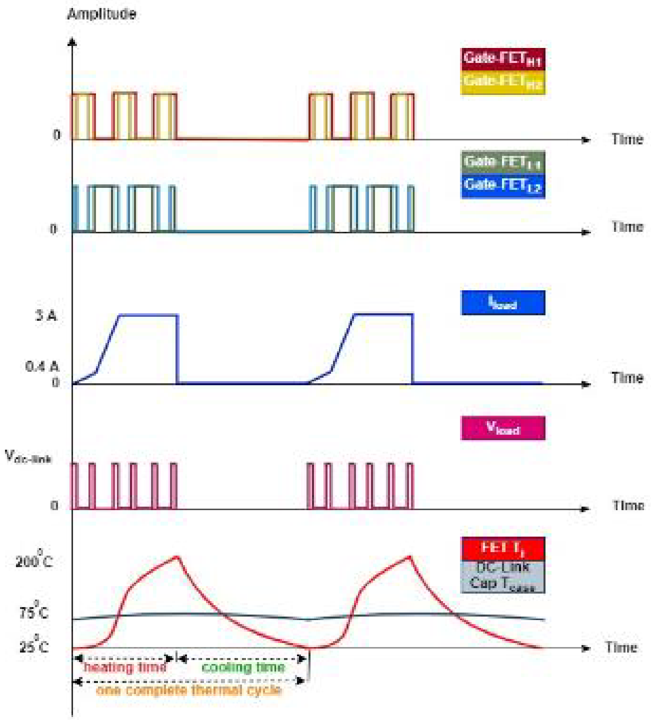


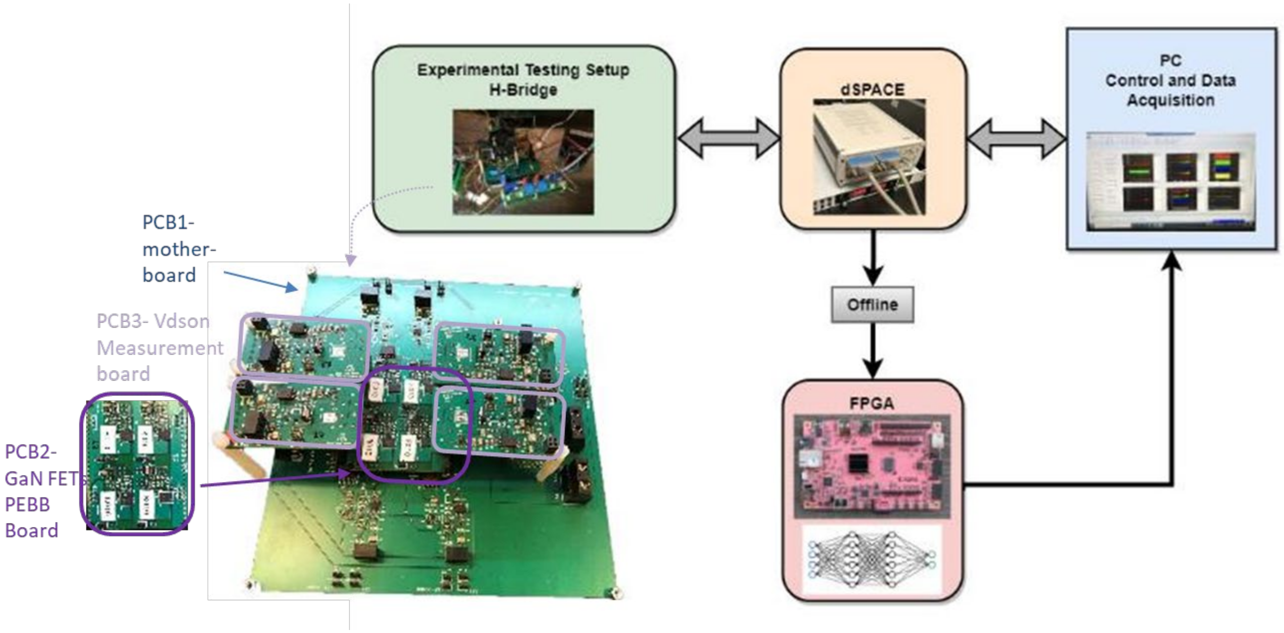
A. Sadat and H. S. **Krishnamoorthy**, "Measure Theory-based Approach for Remaining Useful Lifetime Prediction in Power Converters," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA

System-level Prediction of Probability of Survival



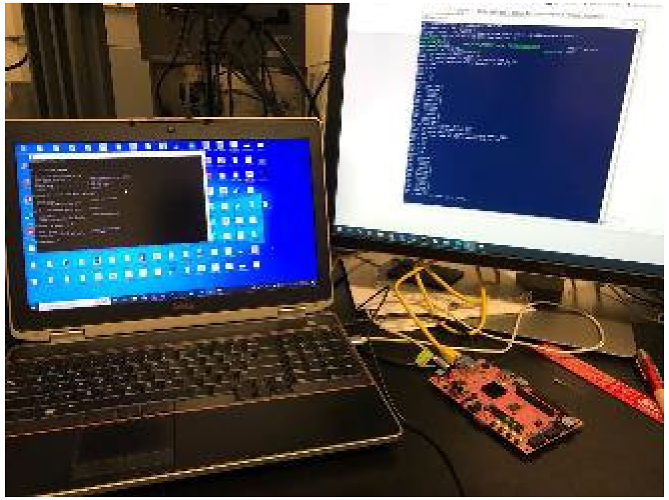


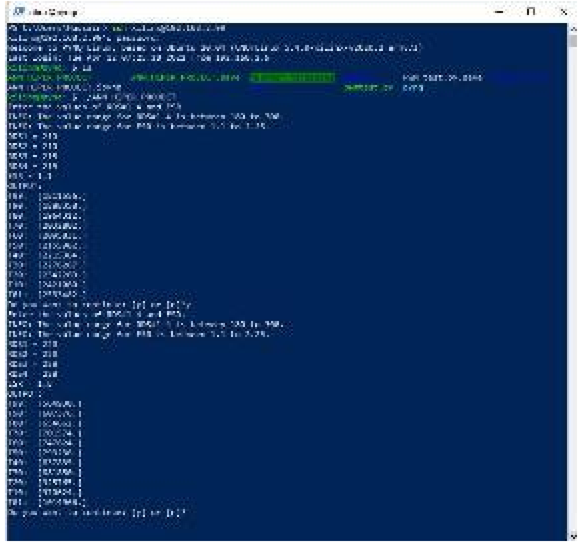


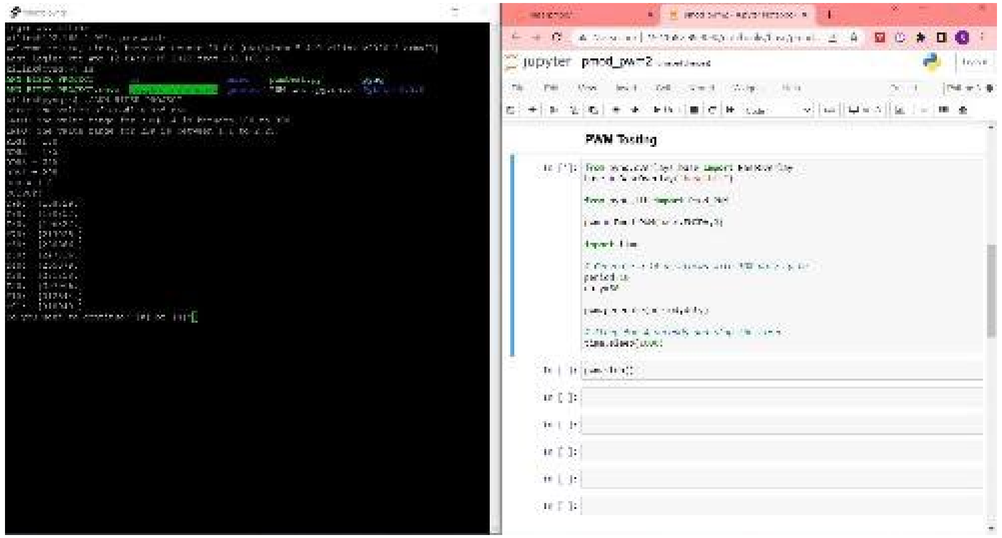


System-level hardware connection and data processing.

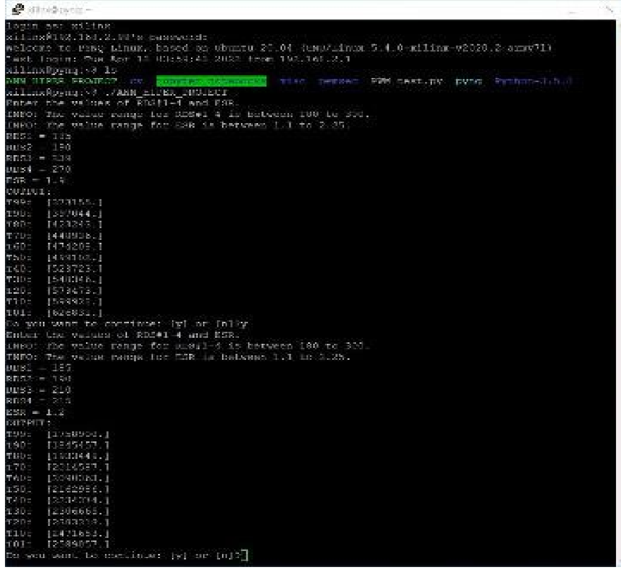
In-Situ Implementation and RUL Estimation

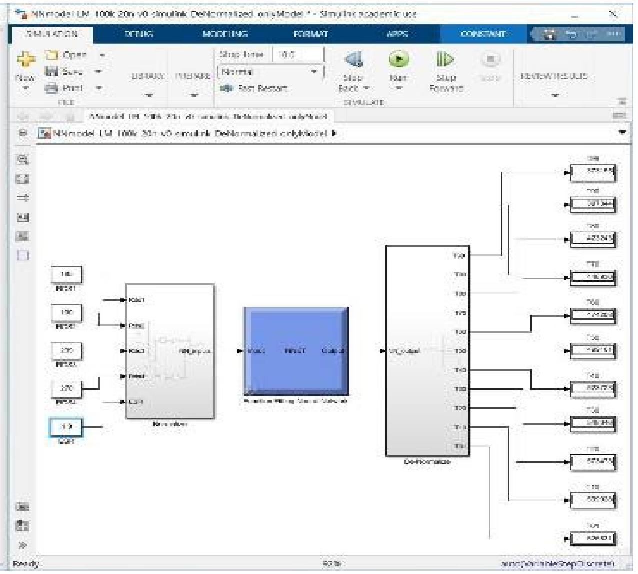


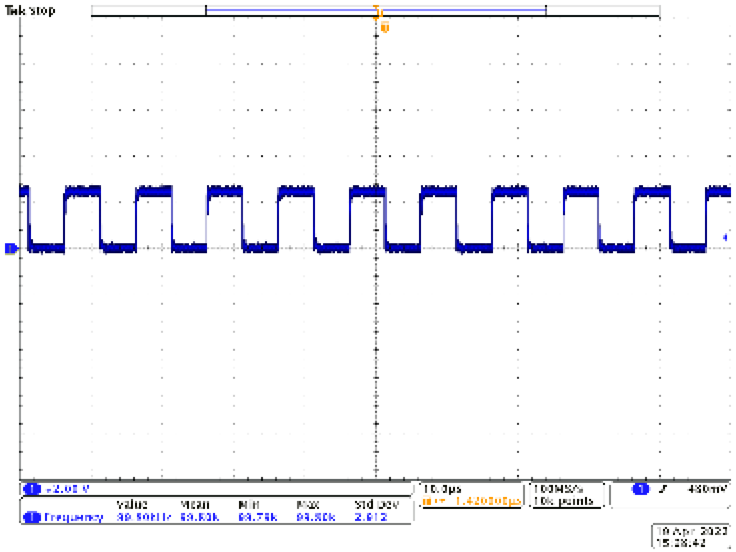




FPGA hardware setup with deployed ANN model for RUL prediction







Summary

- Versatile test setup for parallel accelerated thermal cycling tests for FETs.
- Time constant of sensors is very critical, especially when testing GaN FETs.
- The effective activation energy is affected by the auxiliary components, packaging, accelerated electro-mechanical stresses, etc.
- The degradation of the GaN HEMT is caused by hot-electron trapping, as well as the reduction of mobility and density of carriers in the 2DEG layer.
- ANN model prediction matched the actual experimental results with an error of less than **0.5 %** over a period of 10 % of operational life at high-temperature thermal cycling; enabling in-situ RUL estimation.

Mission Profile–based Health Estimation: For a Longer Converter Life!

DEPARTMENT OF DEFENSE
UNITED STATES OF AMERICA

Thank You!

Dr. Harish Sarma Krishnamoorthy
(Email: hskrishn@uh.edu; Web: http://pemsec.ece.uh.edu/)

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Partners and Collaborators:

Gnana Kulothungan (UH)	Joshua Hawke (U.S. NSWC)
Hussain Sayed (UH)	Amitava Das (Tagore Tech.)
Bharat Bohara (UH)	Amin Sadat (UH)

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