Sandia National Laboratories

Exceptional service in the national interest

# 2.5D HI Packaging of the Power Converter using TSV interposer.

Helen Chung, Andrew Ian Young, Brianna Klein, Matt McDonough, Jason Neely.

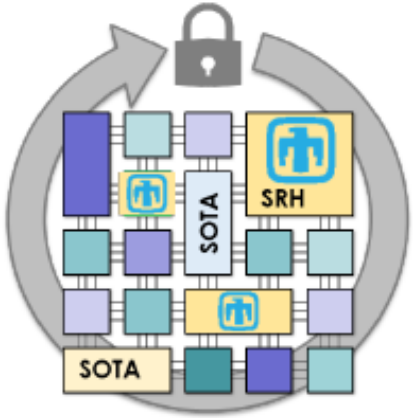
Power Electronics & Energy Conversion Workshop

August 2nd – 3rd, 2023

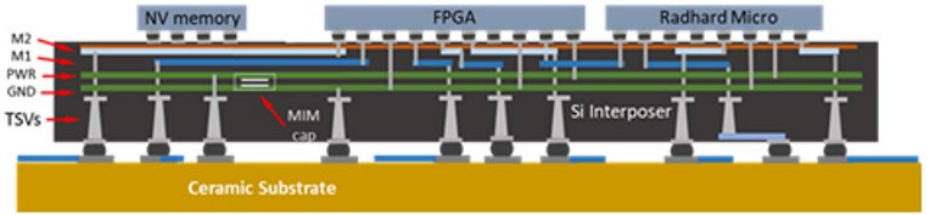
R&A # 1717169

# Purpose and Motivation:

2.5D Integration Fabrication Techniques for a Modular Radiation Resilient Platform




The **2.5D Program** will develop SNL's capability for 2.5D and HI Integration, for flexibility and adaptability in design/manufacturing.



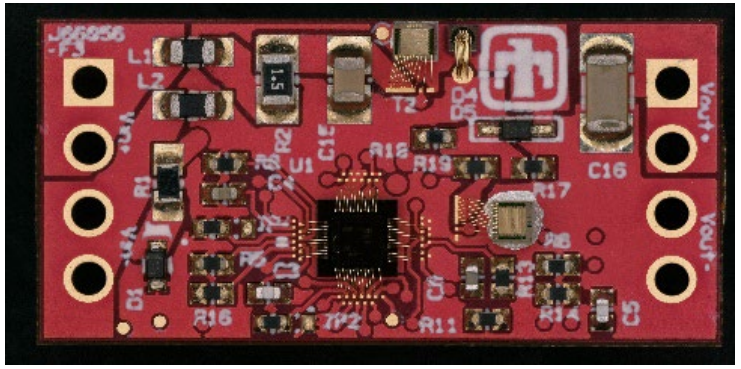

**Heterogenous Integration (HI)** refers to the integration of separately manufactured components into a higher level assembly that provides enhanced functionality and improved characteristics (e.g. flexibility).

# 2.5D Heterogeneous Integration Packaging of

## Radiation Resilient Power Converters

### Power Converter GEN 1

26.7mm

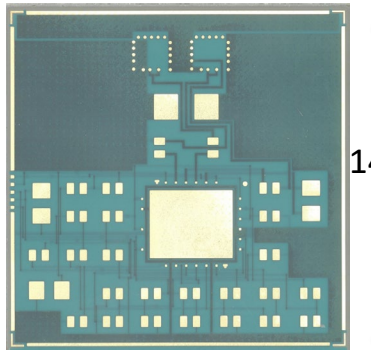


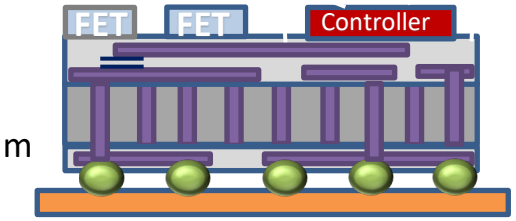
- PCB board
- Components Surface mounted
- Integrated circuits and Power devices wire-bonded

**66% Areal reduction**

### Power Converter GEN 2

13.4mm



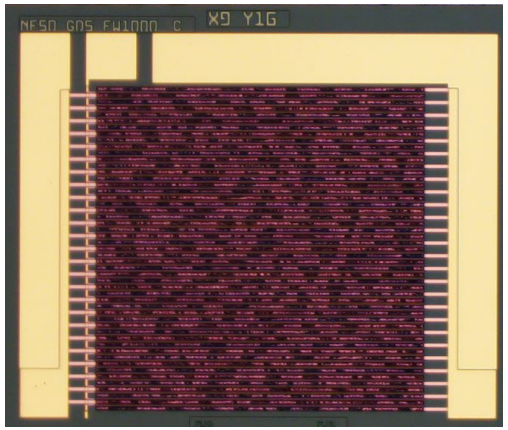




2.5D Heterogeneous Integration with a TSV Interposer

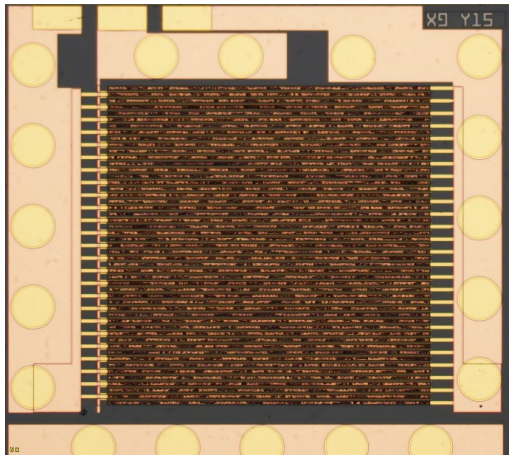
- Smaller foot print (66% areal reduction)→ high power density
- Ease of assemble & part count reduction
- I/O from the bottom of TSV interposer → Lower parasitic inductance versus wire bonds, and potentially higher speed.

# Flip chip

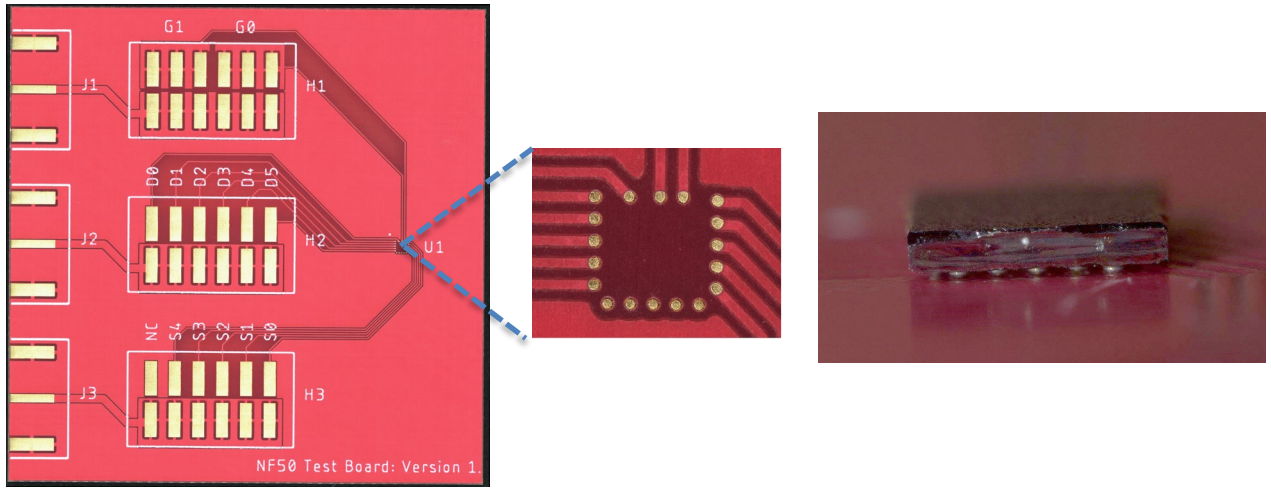
## Standard Layout



## Flip Chip Layout

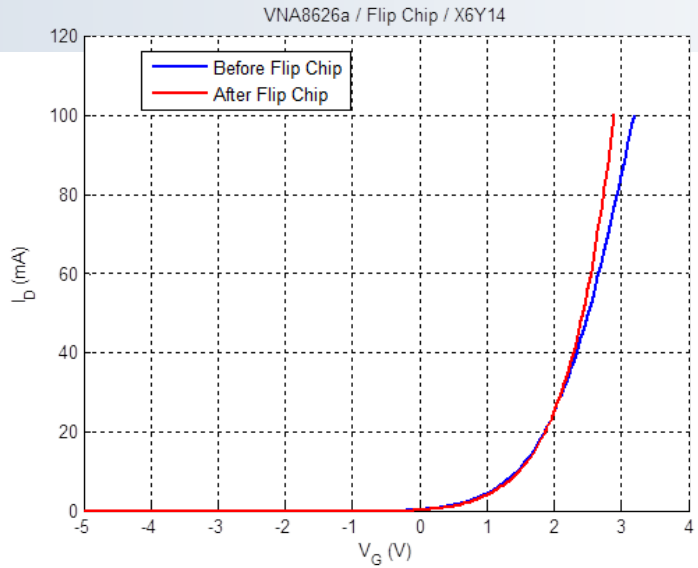


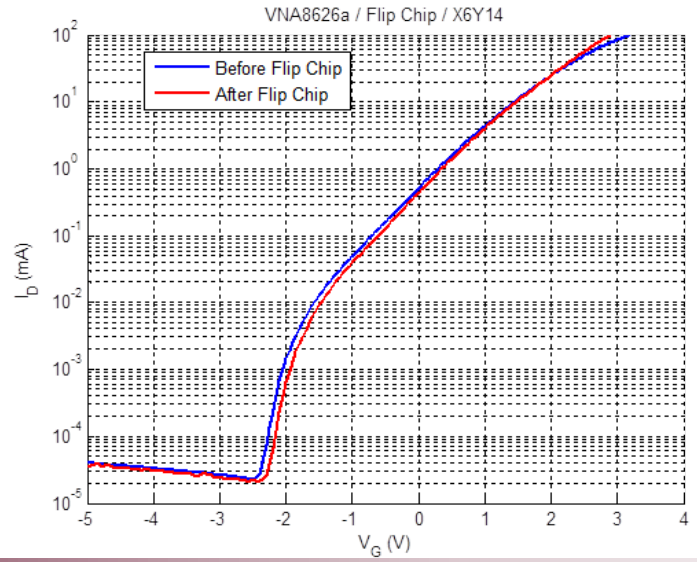
## Flip Chip Test Board








- Observed increased drain current after flip- chip
- Possibly due to increased number of contact points to chip
- Reduced parasitic resistance

Sandia National Laboratories

# Si Core Substrates with TSV (Through Si Via)

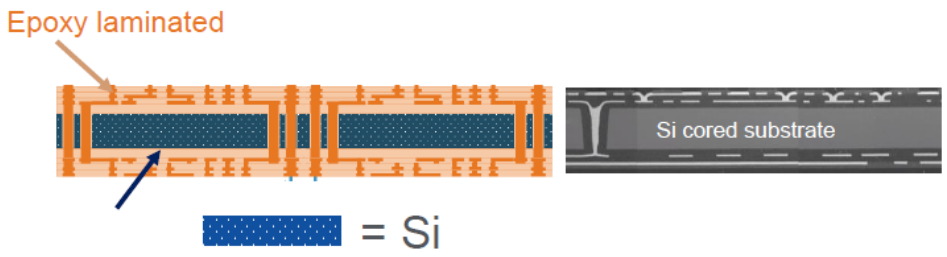
## Basic Idea: Instead of Woven Glass Fiber Mat/Epoxy, use Si as the Rigid Core and Embed in Epoxy

**Cored Substrate**

Printed Circuit Board Like Substrate

GLASS FIBER EPOXY


Si CORE




**Si Core Value**

1) Stiffer

2) Homogenous

3) Creep and Plastic Deformation Free – Fully Elastic

4) Dimensionally Stable

5) Heat Conductive

6) CTE matched with Si die

**Si Core Substrates offer Stiffer Core/die CTE matched/ Heat Conductive/ High Via density/ High Density build-up**

APPLIED MATERIALS

Sandia National Laboratories

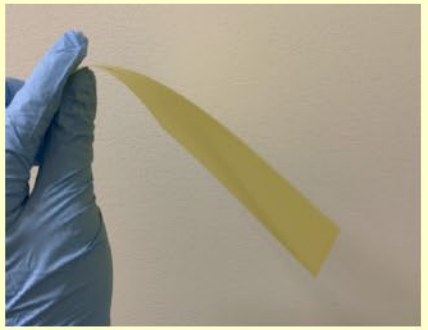
# Si Core Substrates with TSV (Through Si Via)

## Si Core vs. Reinforced Epoxy Core on Stiffness

**Fiber Glass Reinforced Epoxy Core**

- Flexible
- Wavy surface
- Warps

**Thin Reinforced Epoxy Core (140um)**

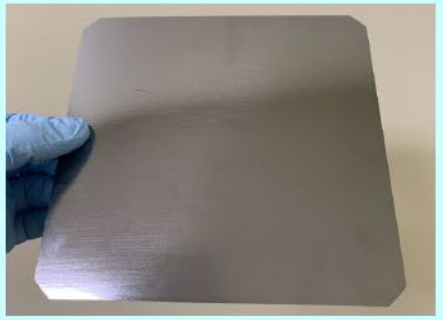


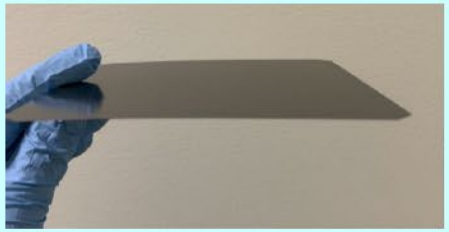
Note: epoxy mold (without epoxy fiberglass web)
Even more flexible

**Si Core**

- Stiff
- Planar
- Doesn't warp

**Thin Si Substrate (110um)**



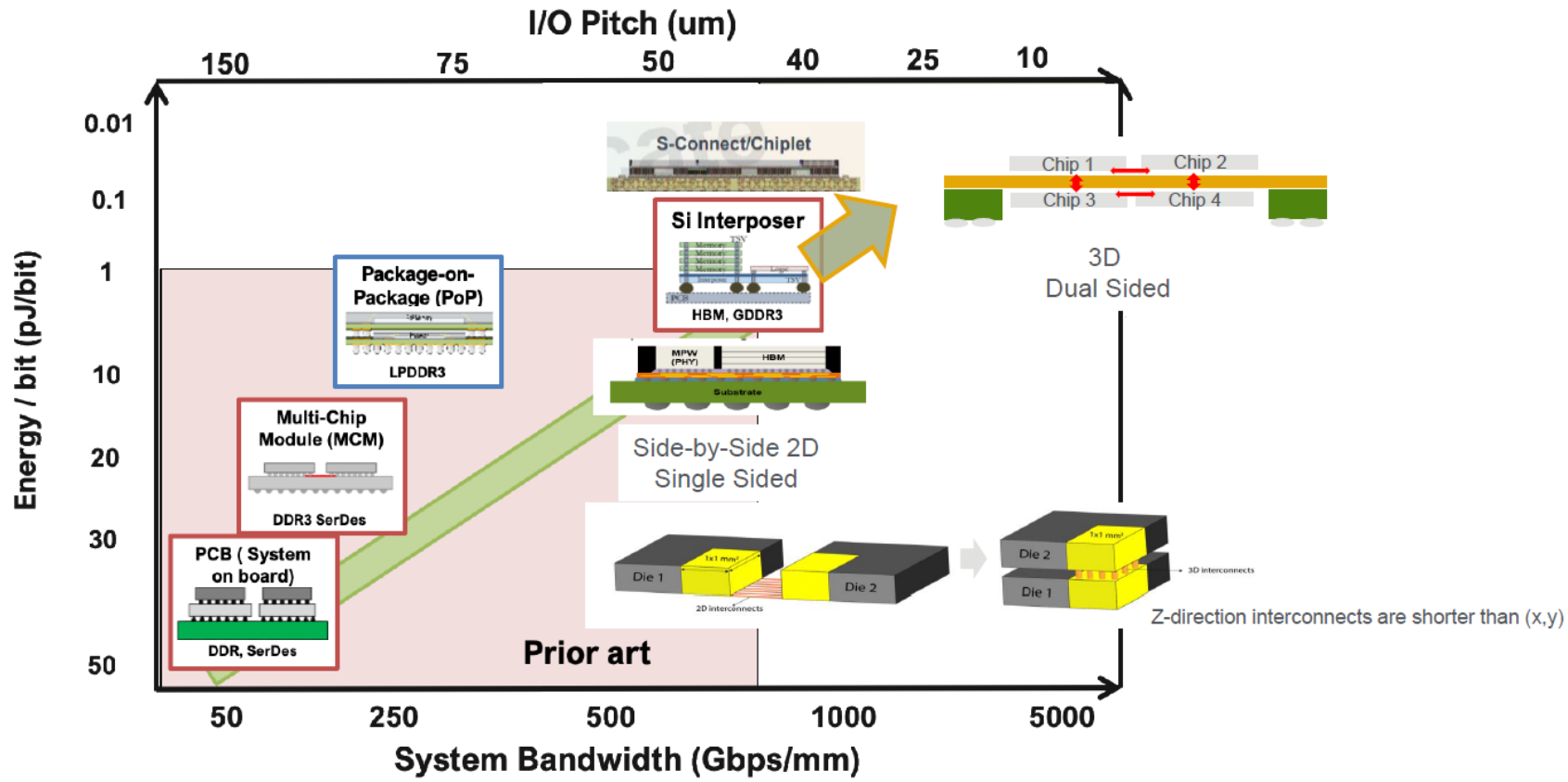


APPLIED MATERIALS

Sandia National Laboratories

# Si Core Substrates with TSV (Through Si Via)

## System Performance Drives Need for 3D Dual Sided Chips

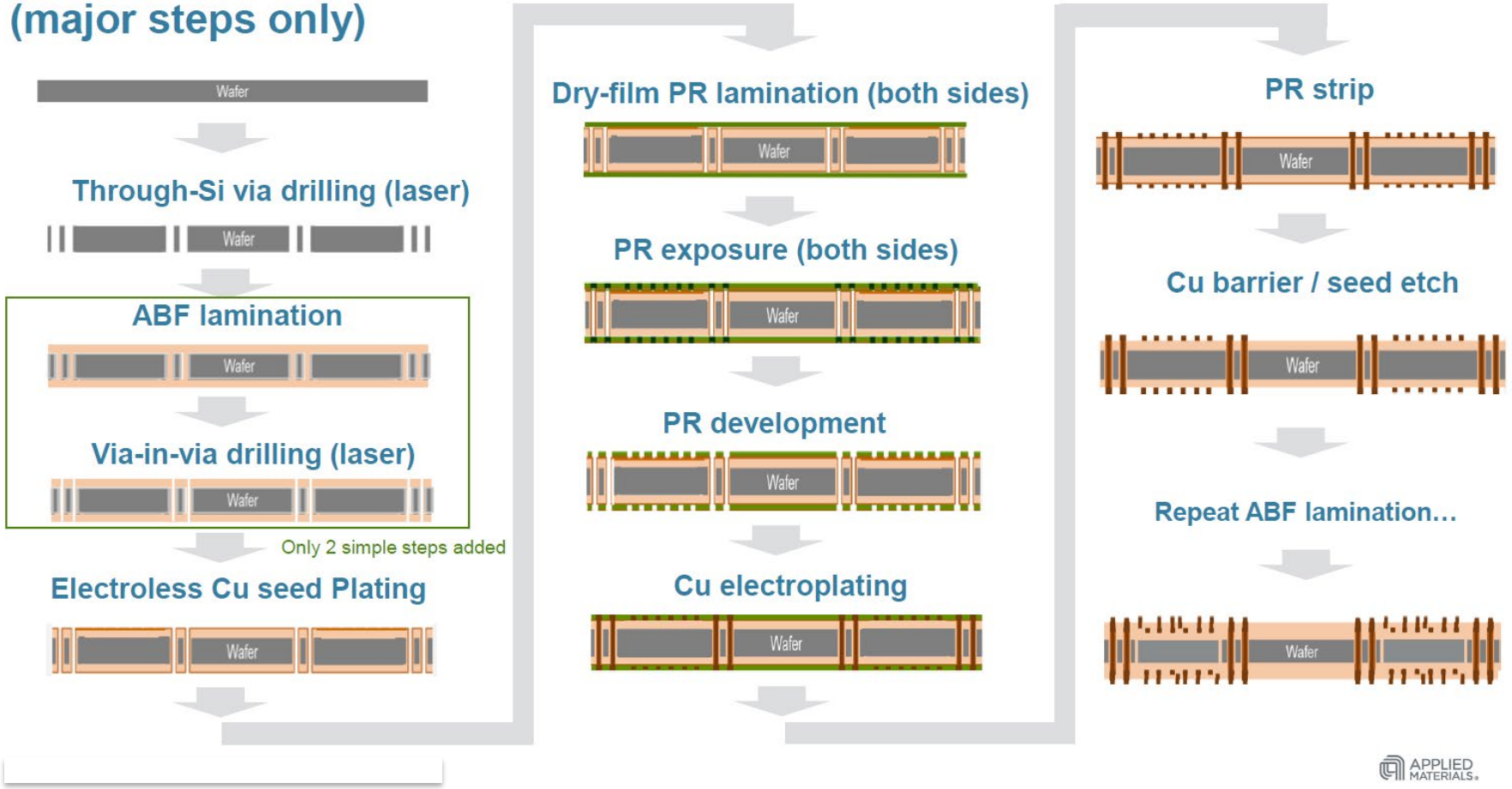



APPLIED MATERIALS

Sandia National Laboratories

# Si Core Substrates with TSV (Through Si Via)

## Si-cored Substrate Process Flow: 2 simple steps added to Laminate Flow (major steps only)



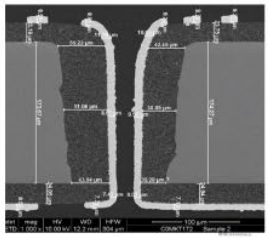

APPLIED MATERIALS

Sandia National Laboratories

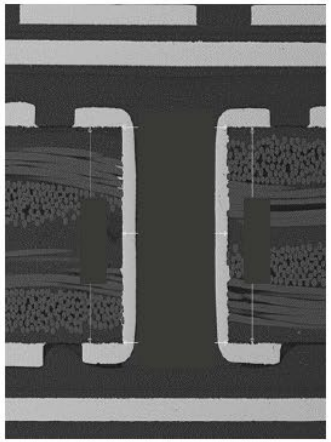
# Si Core Substrates with TSV (Through Si Via)

## Key Technology

Through Si core/Epoxy Via



Through Glass Fiber/Epoxy Via



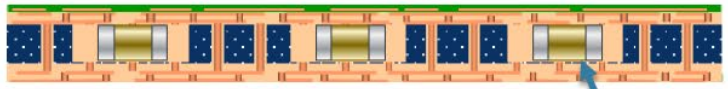
## Configuration Examples

1

Structured Silicon Core + Via-in-Via + RDL

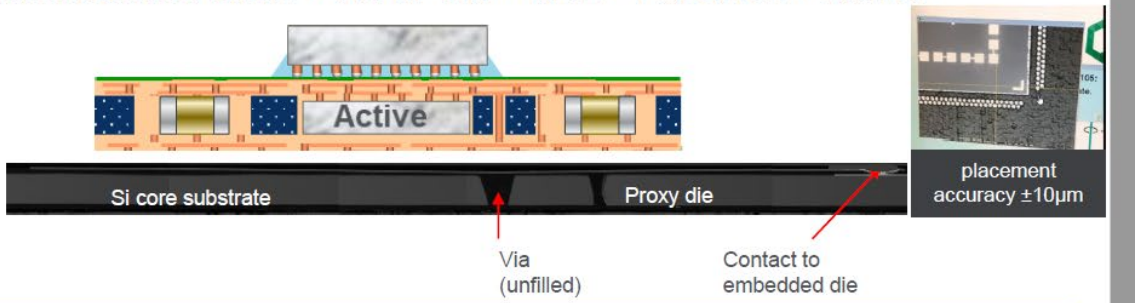

2

Structured Silicon Core + Via-in-Via + RDL+ Passives




3

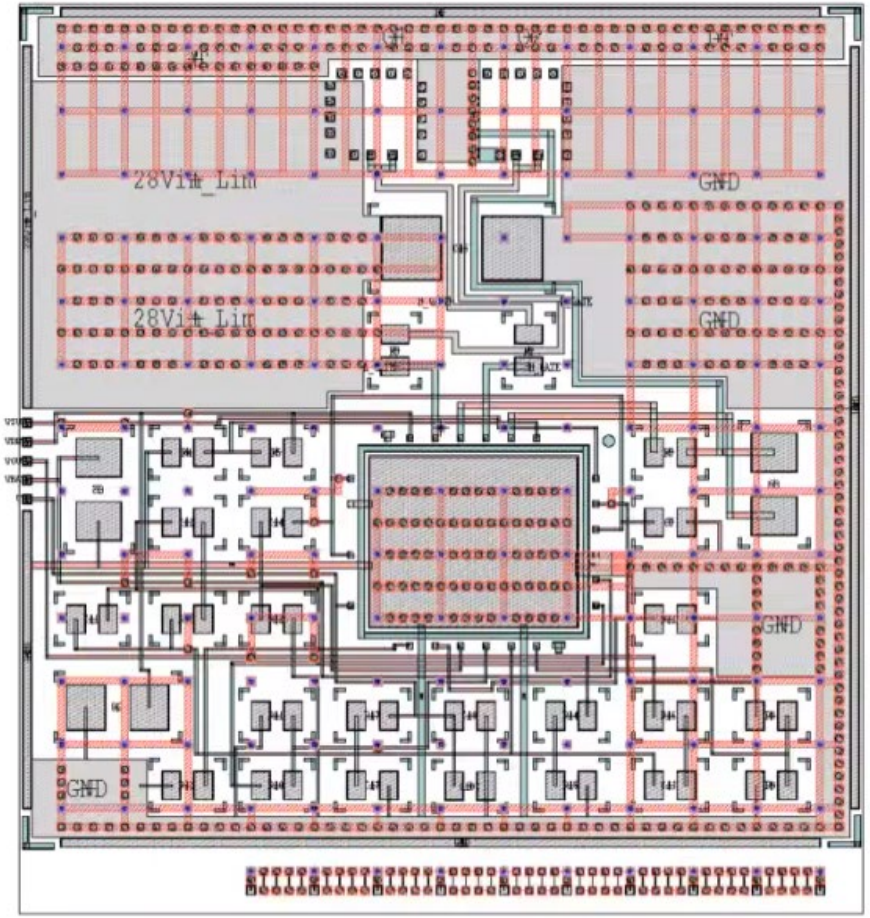
Structured Silicon Core + Via-in-Via + RDL + Passives + Active

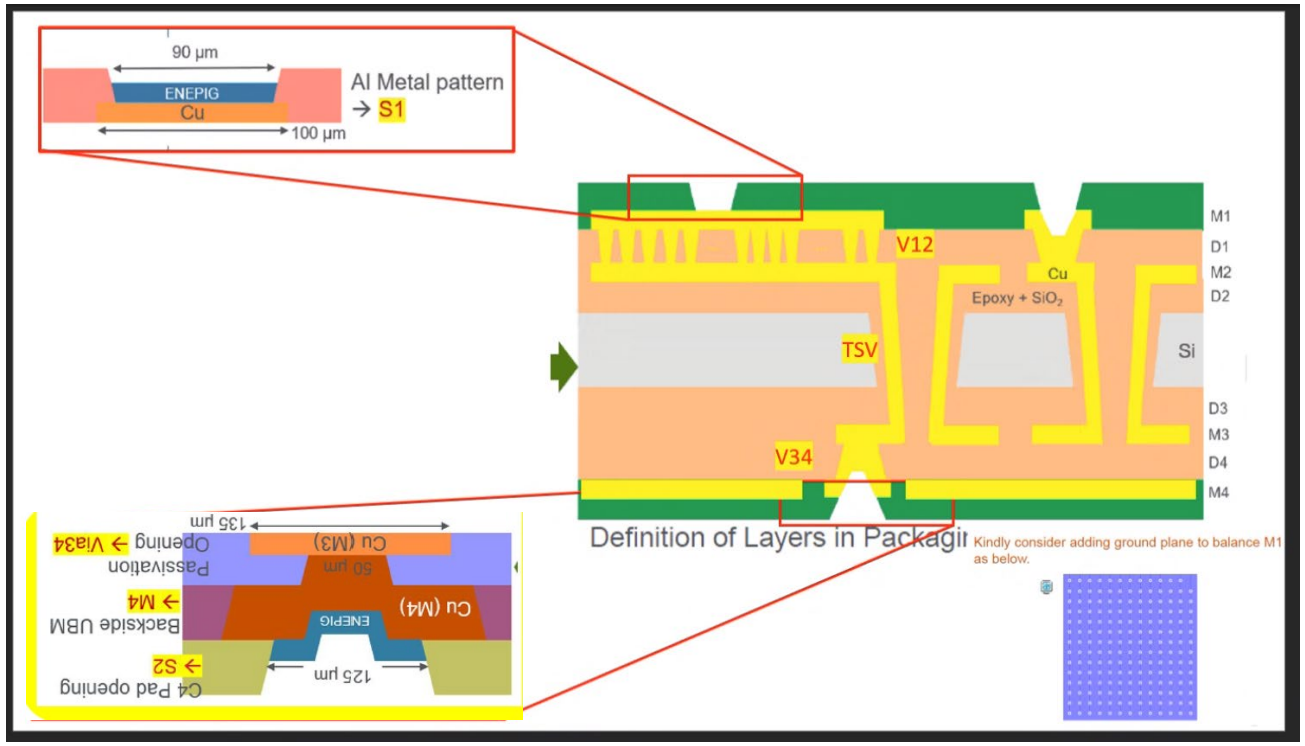



**Enabling Unit Technology is the Through Core Via with Epoxy Lining Formation – Using Mature Metallization process**

# :2.5D HI TSV Interposer fabrication

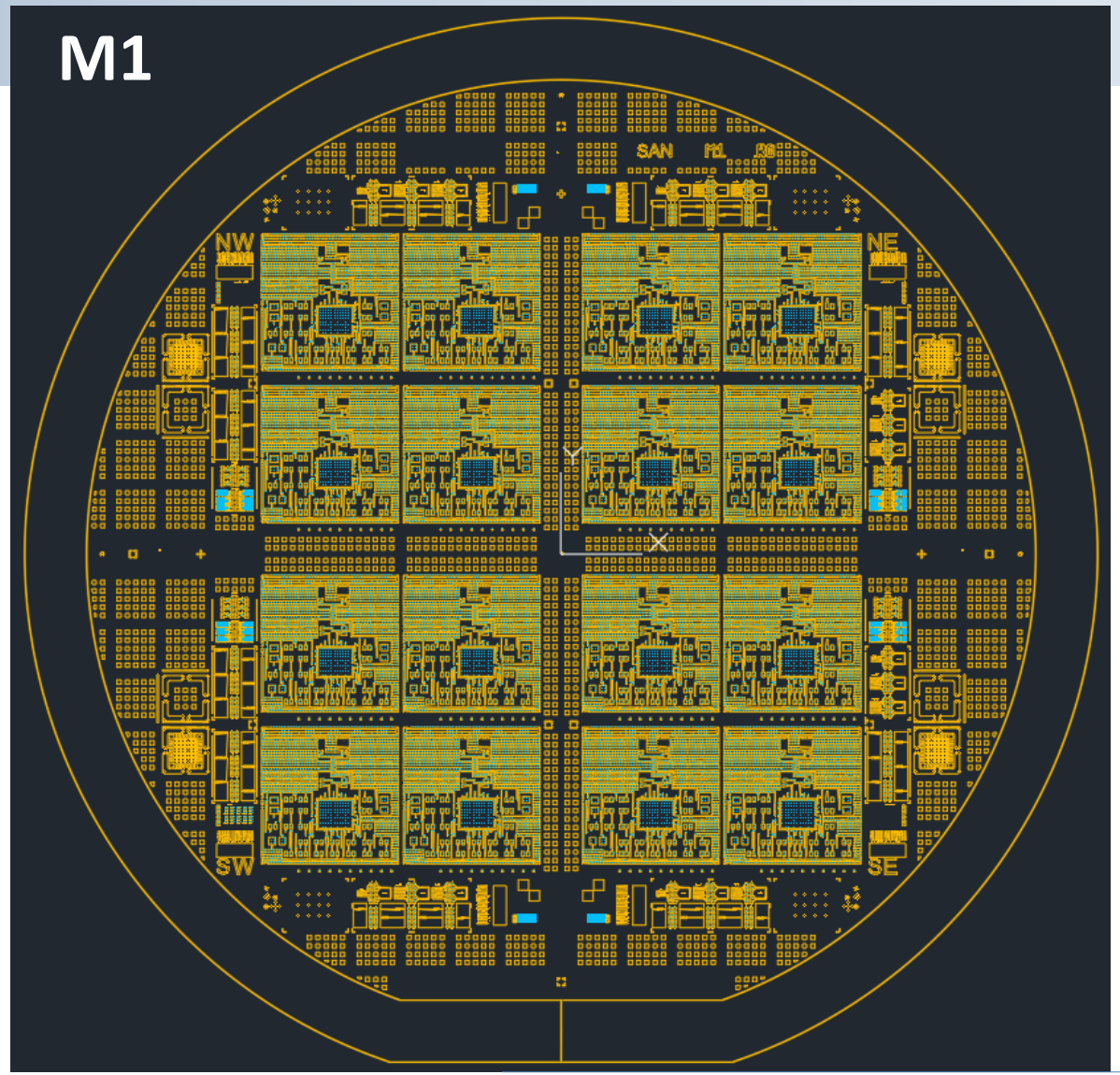
## Power converter: TSV interposer design

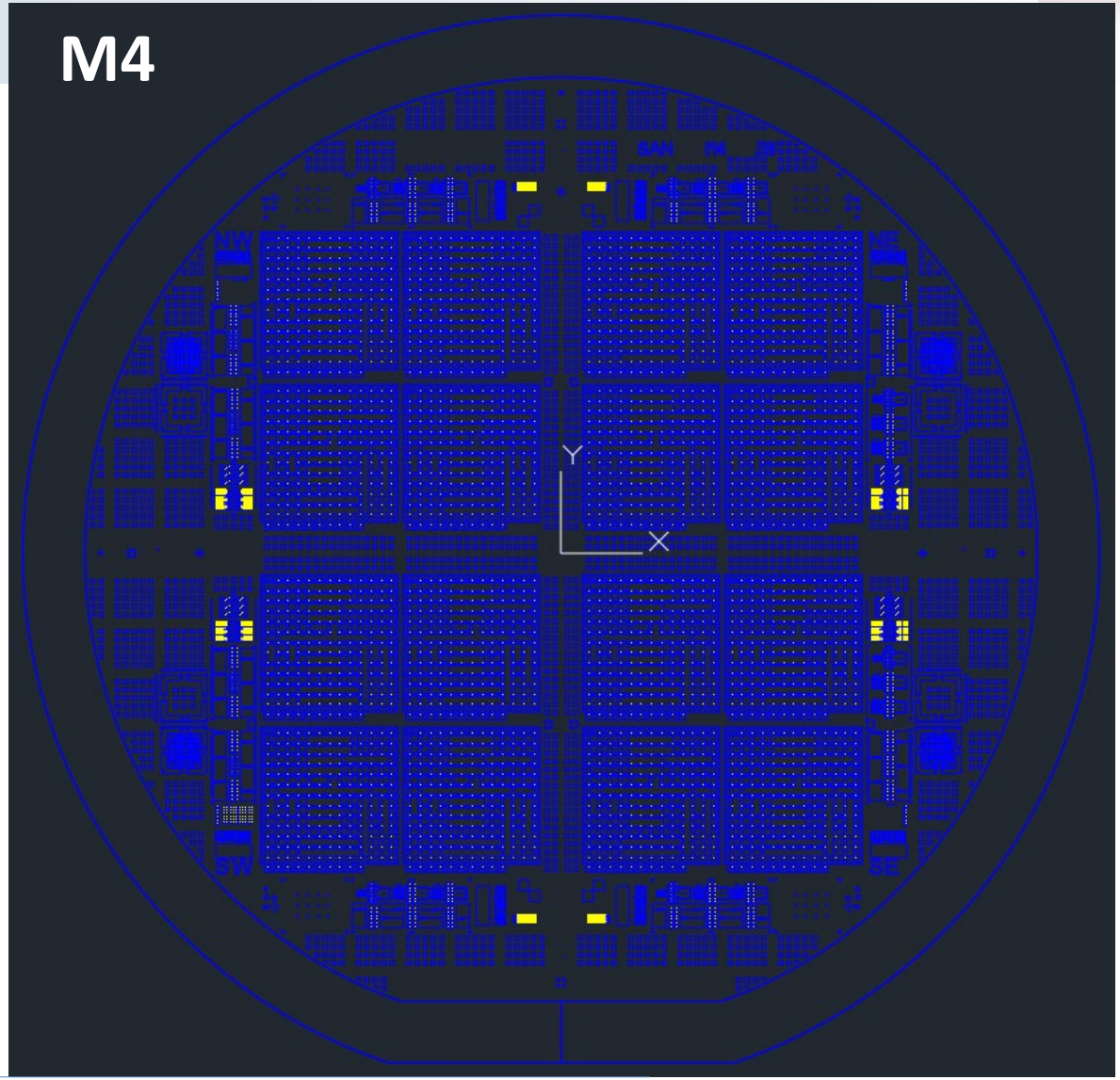



TSV 50um dia. 100um spacing, TSV height 180um.
40um line, 50um spacing.

# Sandia Substrate Layout on Full Wafer

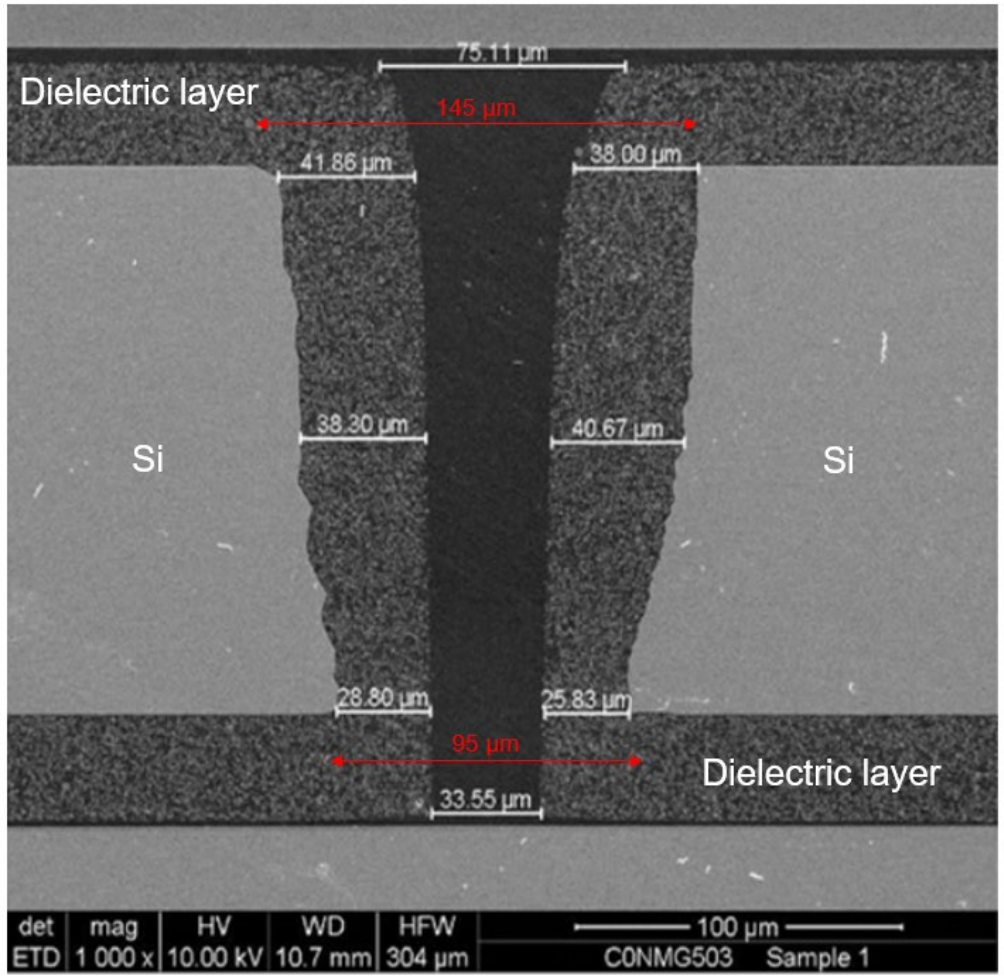


Sandia National Laboratories

# TSV interposer microstructure analysis

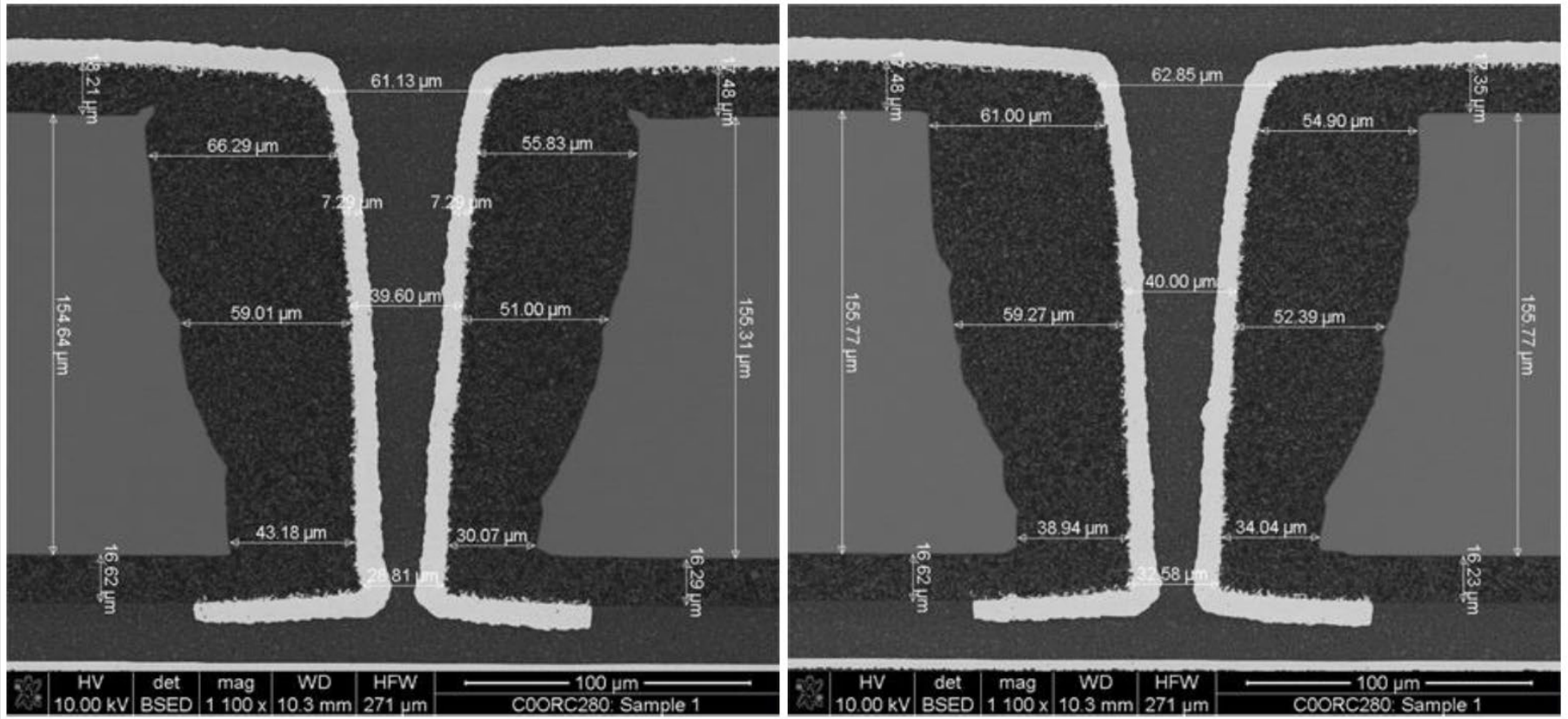
## Via-in-via | Cross-sectional view



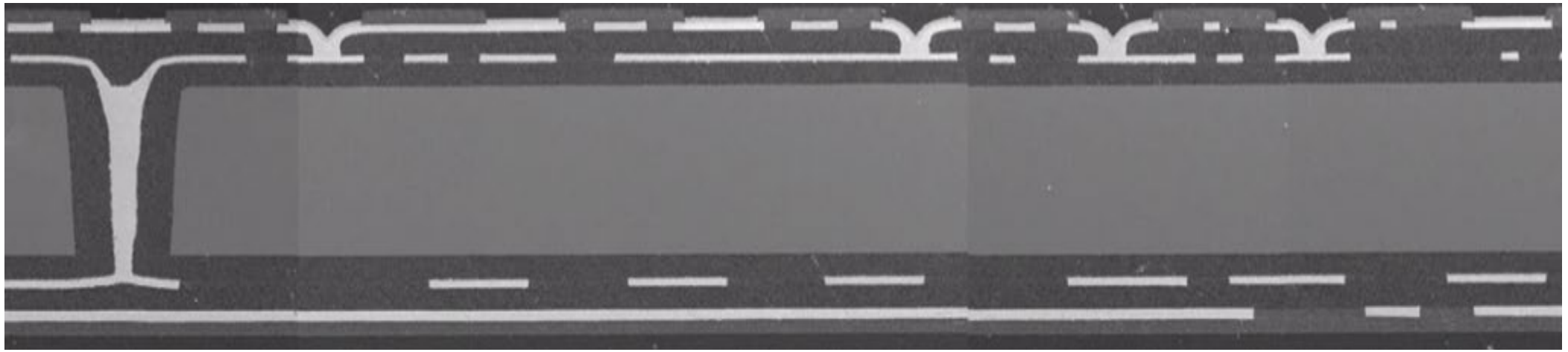
Sandia National Laboratories

# TSV interposer microstructure analysis

## X-SEM Analysis | Via-in-via: Substrate #15



X-SEM of M1/M2/TSV/M3/M4
(more measurement data will be delievered by 5/26/23)

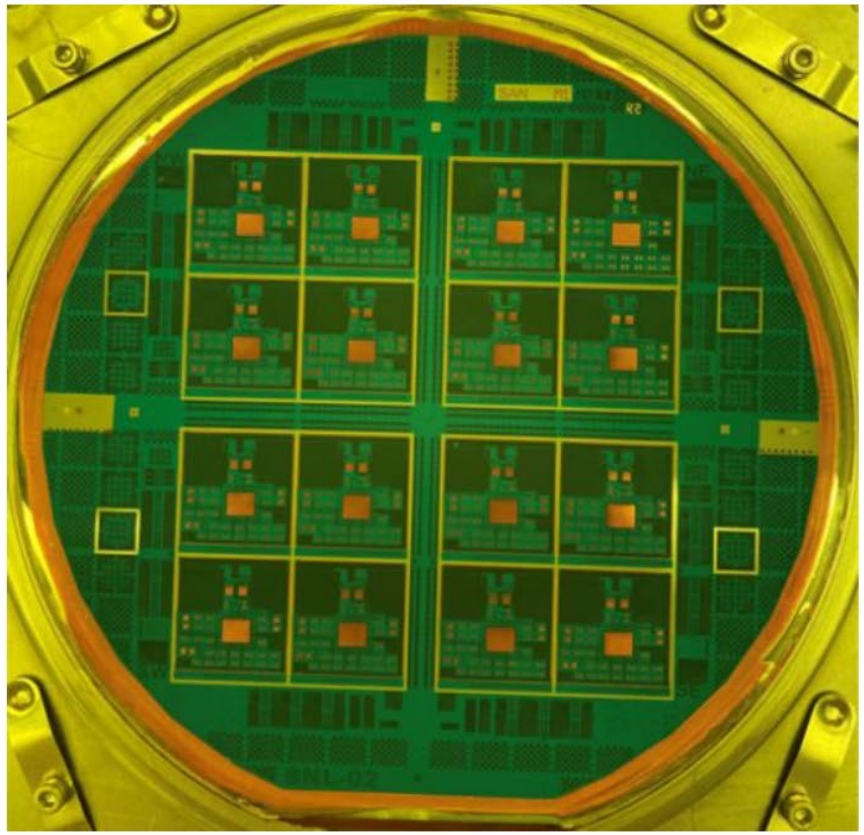


Sandia National Laboratories

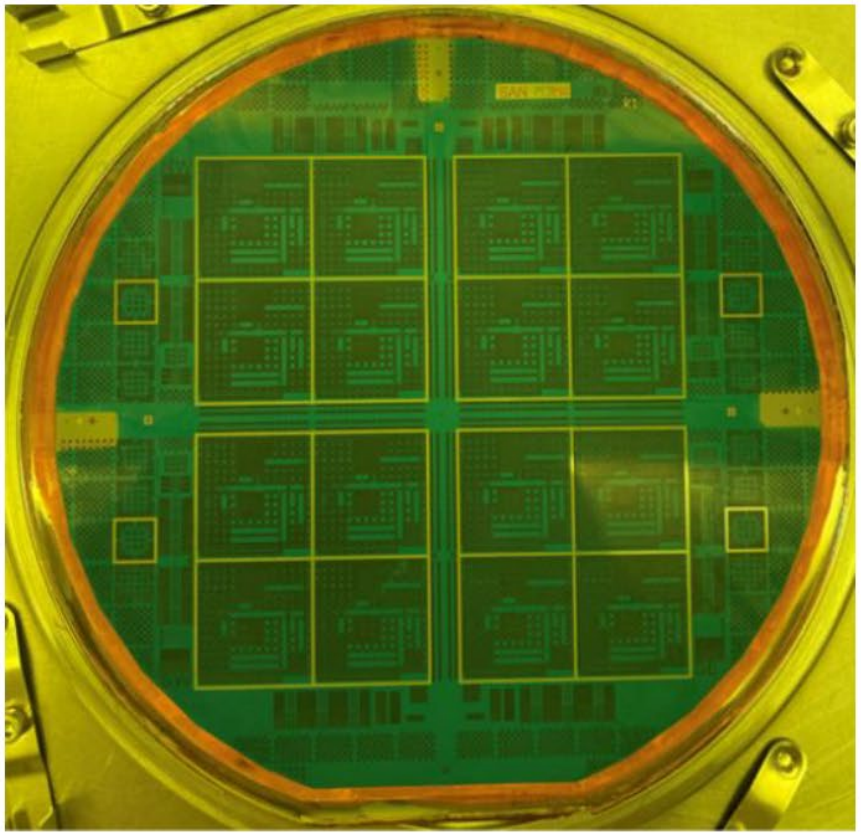
# Si Core Substrates with TSV (Through Si Via)

## Solder Mask | SNL-02

Front side



Backside

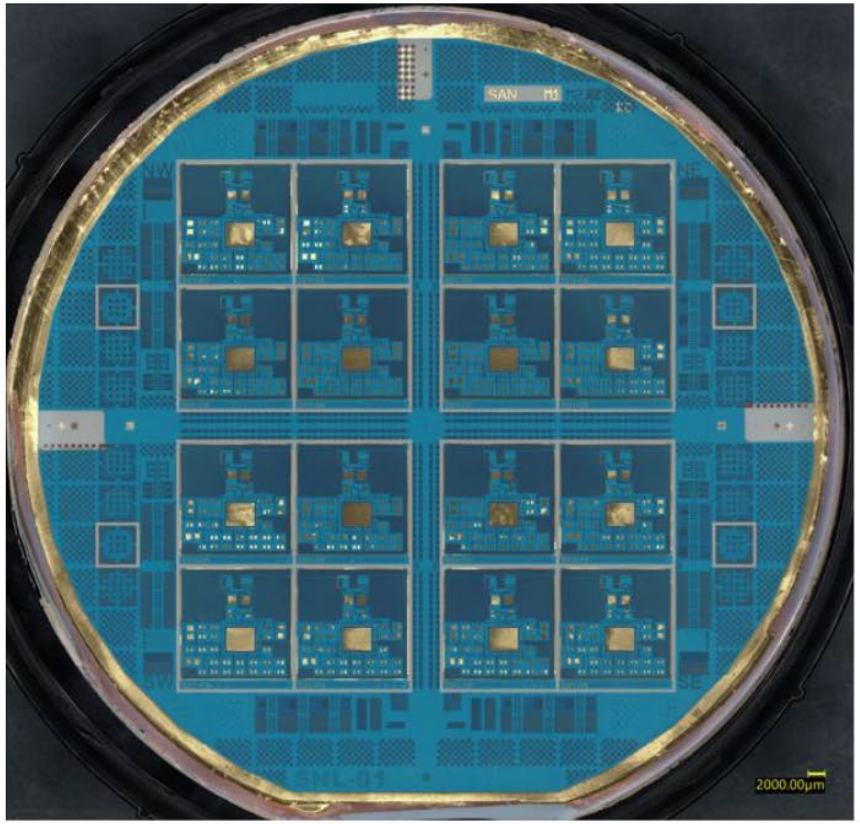


Sandia National Laboratories

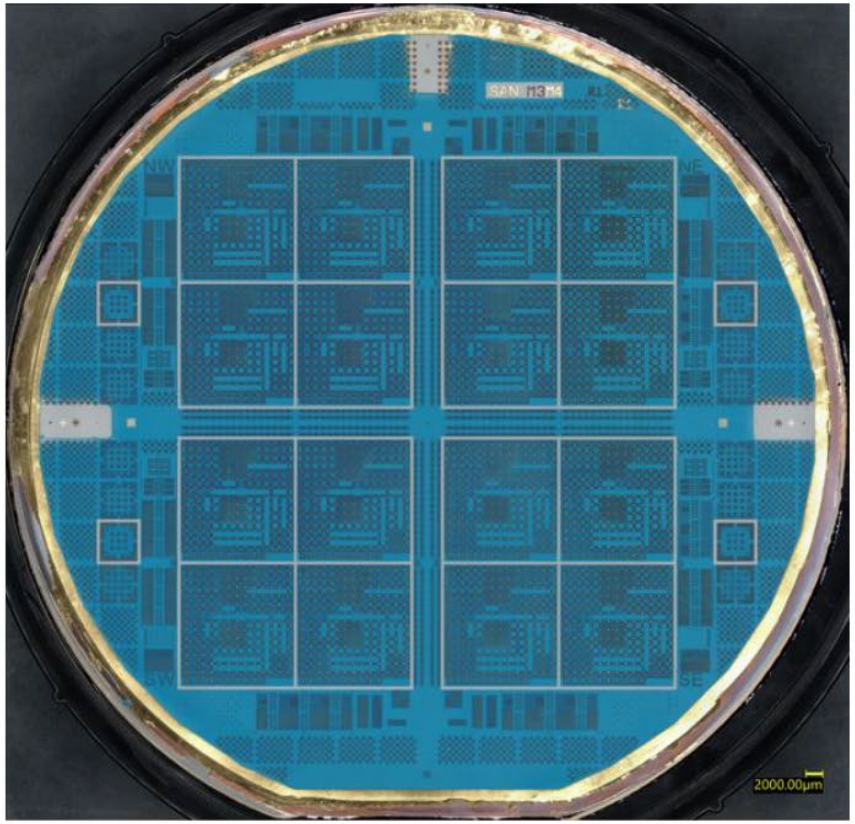
# Si Core Substrates with TSV (Through Si Via)

## ENEPIG | SNL-01

Front side

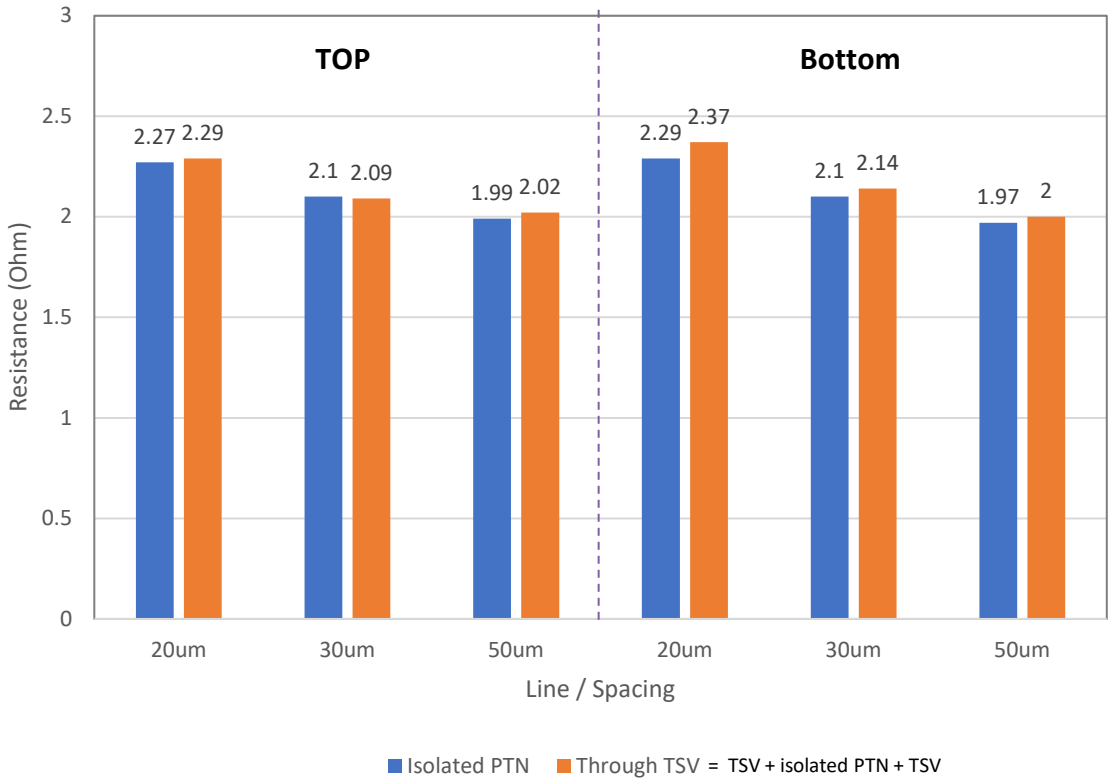



Backside

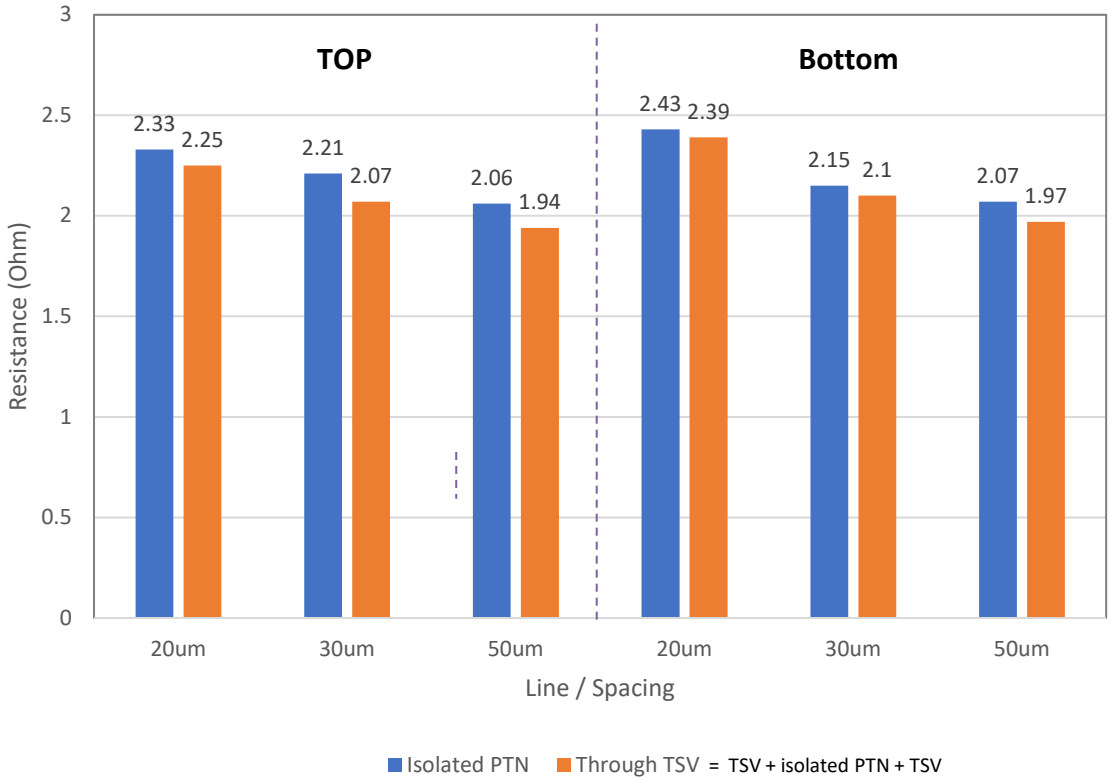


# Resistance of M2/M3 Applied Materials PCM l SNL-02

## M2 Daisy-chain PCM Pattern




## M3 Daisy-chain PCM Pattern



Sandia National Laboratories

# Si Core Substrates with TSV : Reliability test

## Reliability Results of TSV Chains | Applied 2C2 Build

Initial

| Outer TSV | Inner TSV |
|---|---|
| 1.41 | 1.56 |
| 1.38 | 1.53 |
| 1.40 | 1.55 |
| 1.39 | 1.53 |
| 1.44 | 1.59 |
| 1.51 | 1.66 |
| 1.49 | 1.67 |
| 1.48 | 1.64 |
| 1.50 | 1.65 |
| 1.48 | 1.60 |
| 1.43 | 1.54 |
| 1.54 | 1.67 |
| 1.47 | 1.60 |
| 1.43 | 1.59 |
| 1.50 | 1.64 |
| 1.55 | 1.71 |
| 1.50 | 1.65 |
| 1.52 | 1.67 |
| 1.49 | 1.63 |
| 1.43 | 1.56 |
| 1.43 | 1.59 |
| 1.41 | 1.59 |
| 1.42 | 1.58 |
| 1.40 | 1.55 |

MSL3 Pre-Condition:
Bake, @125°C for min. 24 hours
Soak, @30°C, 60%RH for 192 hours
x3 Reflow, @260°C

| Outer TSV | Inner TSV |
|---|---|
| 1.4 | 1.55 |
| 1.37 | 1.53 |
| 1.4 | 1.54 |
| 1.38 | 1.51 |
| 1.43 | 1.58 |
| 1.5 | 1.65 |
| 1.48 | 1.66 |
| 1.46 | 1.63 |
| 1.49 | 1.64 |
| 1.46 | 1.59 |
| 1.42 | 1.54 |
| 1.49 | 1.65 |
| 1.46 | 1.59 |
| 1.42 | 1.56 |
| 1.49 | 1.63 |
| 1.54 | 1.7 |
| 1.48 | 1.64 |
| 1.51 | 1.66 |
| 1.48 | 1.62 |
| 1.42 | 1.55 |
| 1.42 | 1.57 |
| 1.41 | 1.57 |
| 1.41 | 1.57 |
| 1.4 | 1.56 |

After 1000 cycles
-55°C/125°C

| Outer TSV | Inner TSV |
|---|---|
| 1.4 | 1.6 |
| 1.4 | 1.5 |
| 1.4 | 1.5 |
| 1.4 | 1.5 |
| 1.4 | 1.6 |
| 1.5 | 1.7 |
| 1.5 | 1.7 |
| 1.5 | 1.6 |
| 1.5 | 1.6 |
| 1.5 | 1.6 |
| 1.4 | 1.5 |
| 1.5 | 1.7 |
| 1.5 | 1.6 |
| 1.4 | 1.6 |
| 1.5 | 1.6 |
| 1.6 | 1.7 |
| 1.5 | 1.6 |
| 1.5 | 1.7 |
| 1.5 | 1.6 |
| 1.4 | 1.6 |
| 1.4 | 1.6 |
| 1.4 | 1.6 |
| 1.4 | 1.6 |
| 1.4 | 1.6 |

Both outer and inner TSV chains showed 100% yield after MSL3 and TC1000.

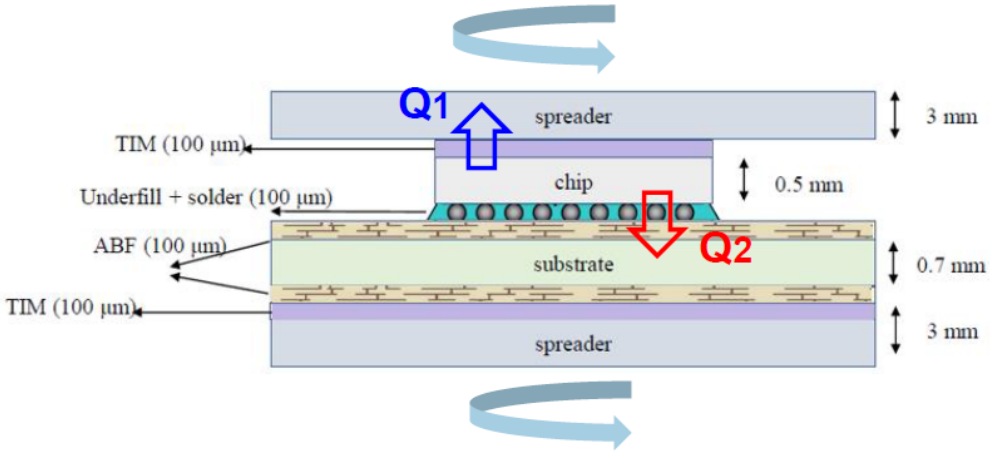
APPLIED MATERIALS

Sandia National Laboratories

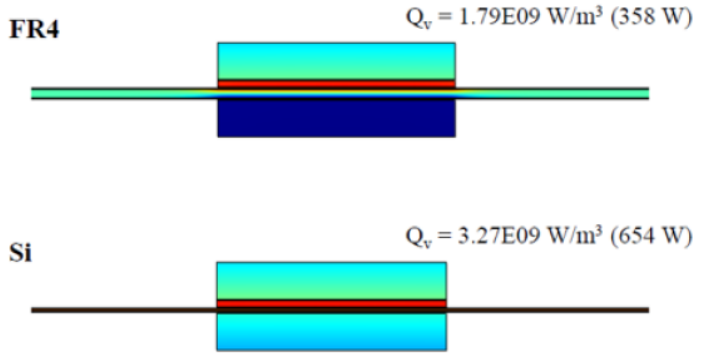
# Si Core Substrates with TSV: Heat dissipation

## Dual-sided cooling allows up to 1.8x higher power output

Convective heat transfer coefficient h = 50000 W/(m²·K)




$T_{max}$ = 70 °C




| Heat Sink | Allowable Chip Power (in Heat Generation) at Maximum Chip Temperature ~70°C | |
|---|---|---|
| Location | Organic substrate | Si substrate |
| Chip-side only | (Qmax)organic = 1x | (Qmax)Si = 1x |
| Dual sided cooling | (Qmax)organic = 1x | (Qmax)Si = **1.8x** |

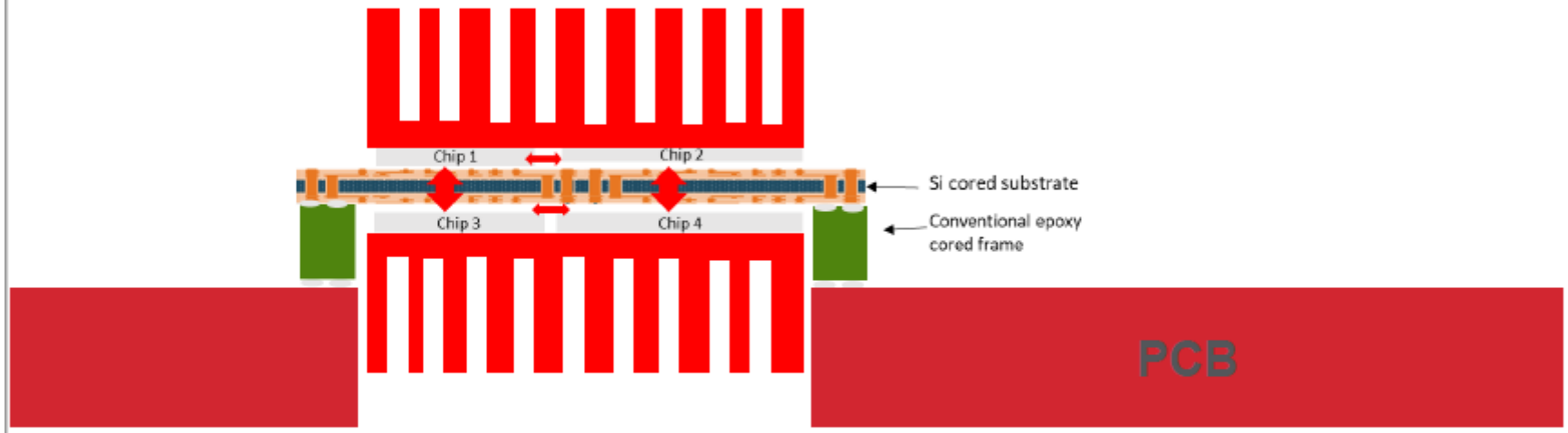
**Dual Sided Cooling possible with Heat Conductive Si Core**

APPLIED MATERIALS

Sandia National Laboratories

# Si Core Substrates with TSV: Heat dissipation

## Full Thermal Access with 3 D Stack face to face.




**Various Ways to Achieve 3D Stacking with both 3D and 2D access and Thermal Access**

APPLIED MATERIALS