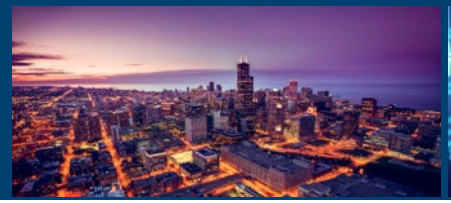
RESILIENT ENERGY SYSTEMS

Mission Campaign



AC to AC Solid State Transformer with Bidirectional Switches

Jack Flicker, Andrew Binder, Jacob Mueller, Todd Monson, Andy Dow, Luciano Garcia-Rodriguez, Richard Floyd, Felipe Palacios

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End Date: 09/30/2026

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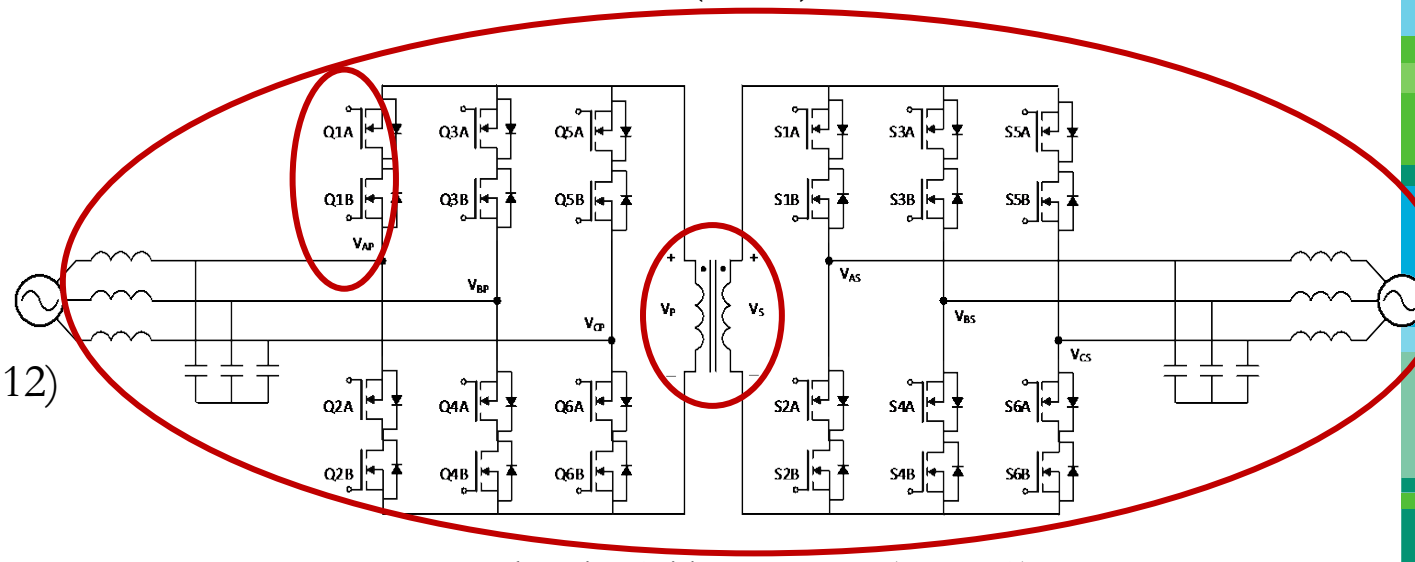
Type I SST with Bidirectional Switches

- ✓ Smaller size/weight compared to Xformers
- ✓ Switching control allow for adaptive protection and power quality enhancement
- ✓ No DC link capacitor
  - → Reliability increase
  - → simpler cascading of modules at higher voltages
- ✓ Bidirectional switches reduce component count (20 to 12)
- ✓ Reduction in physical topology size and complexity
- ✓ Single stage increases efficiency
- X Formidable control complexity

AC/DC-DC/DC (DAB)-DC/AC



AC-AC Dual Active Bridge converter (AADAB)

Fundamental materials and control challenges have limited SST implementation….

Require materials-level improvements

Insert Advanced Materials into operational circuit for comparison to baseline commercial devices

1. AC:AC DAB Circuit Evaluation and Design
2. SiC Bidirecational Switch Design
3. Soft Magnetic Materials

SiC BiDFET Fabrication

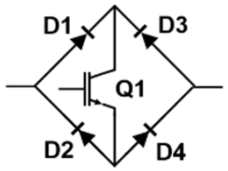
- 4 quadrant operation enables new circuit topologies (CSI, AC:AC SST, etc)
  - Conventional semiconductor unidirectional due to asymmetric layout
    - Up to 5 discrete components to enable 4 quadrant
    - High switching losses/on-state voltage drop (~3.5 V)

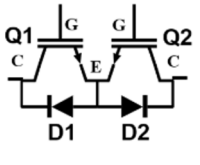
- Monolithic Bidirectional Field Effect Transistor (BiDFET)
  - ✓ Reduce C_{OSS} & C_{RSS} by 2x → increase switching frequency
  - ✓ Low on-state voltage drop (0.5 V)
  - ✗ Not commercially available
  - ✗ Needs better short circuit robustness (SCWT)
  - ✗ Monolithic BiDFET die area is large so yield is low

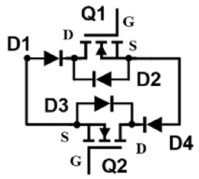
1. Convert established MOSFET design* to BiDFET design
   - Sandia design of devices
   - Fabless process flow for SiC devices

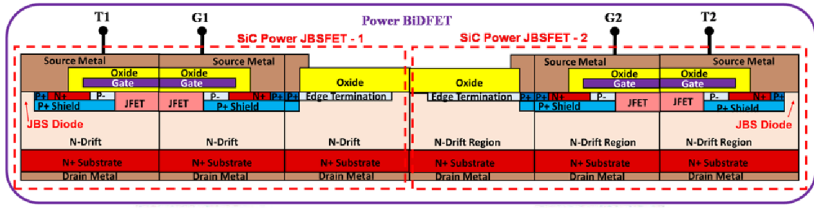
2. Improve short circuit performance using **deep p-well** structure*

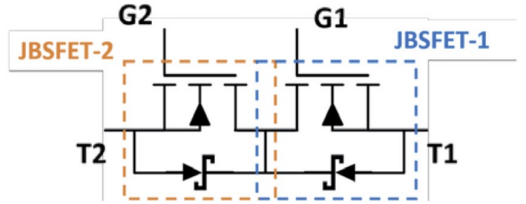
3. Reduce die size by 2x (improve yield, switching frequency) via **channel diode** enabled by deep p-well*

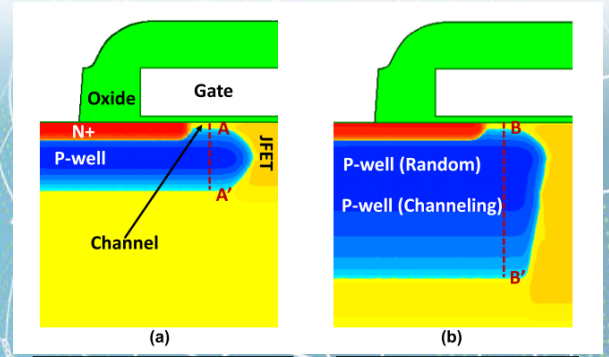












Conventional

Deep p-well

*** In partnership with SUNY Poly**

Soft Magnetic Materials for Transformer Core

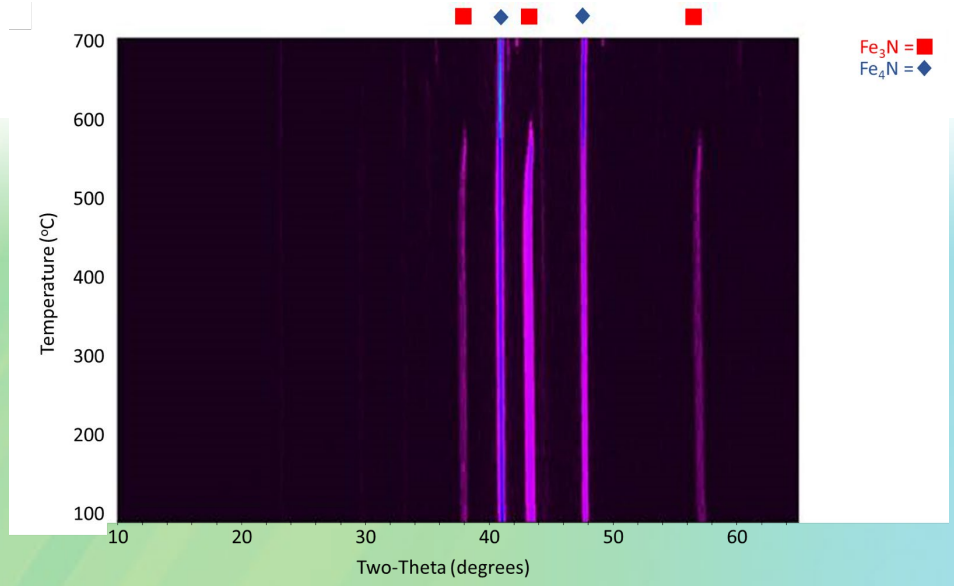
High-frequency magnetic transformers

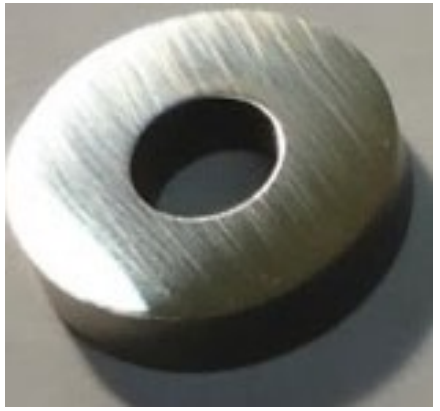
- High power density is required
- Compacted ferrite powders
- Low saturation (J_s< 0.5 T)
- **Severely limits** power density

Soft magnetic phase of iron nitride (γ'-Fe_4N)

- J_s ~ 1.89 T
- Exceeds ferrites by >3x
- Spark Plasma Sintering into arbitrary shapes
- No heavy or rare metals

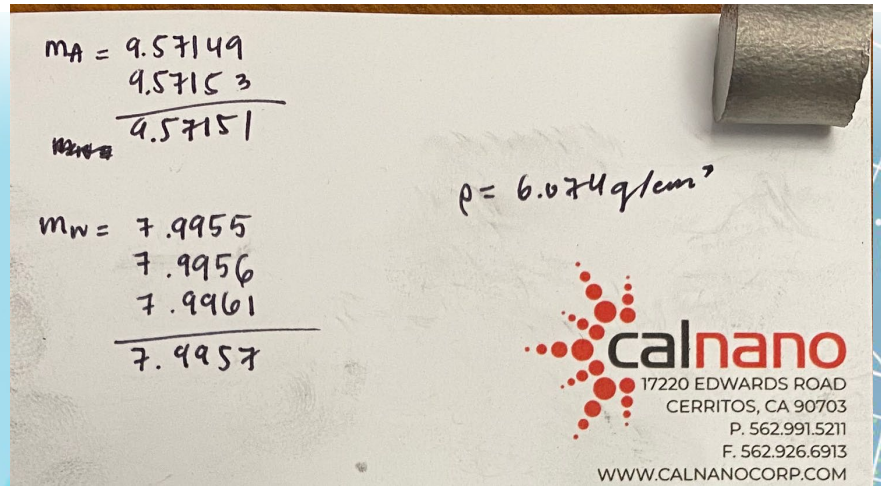
Phase Purification → Ball milling → Core Sintering





Net-shaped toroid (no machining required)

Magnetic Material	J_s (T)	ρ(μΩ·m)	Cost
VITROPERM (Vacuumschmelze)	1.20	1.15	High
Metglas 2605SC	1.60	1.37	High
Ferrite (Ferroxcube)	0.52	$5x10^6$	Low
Si steel	1.87	0.05	Low
γ'-Fe_4N	1.89	> 200	Low



Solid state transformer project roadmap

Circuit Simulation, Design, and Fab

BiDFET Fab

Passive Materials
Magnetics/Capacitors

Year 3

Prototype C
3ϕ, 30 kW
Cascaded Prototype B

- *1.2kV, 50 mΩ (25 A) SiC BiDFETs demonstrated*
- Gen 2 devices evaluated in *Prototype C*

- Fe_4N magnetic core in *Prototype C*

Parallel/Cascaded multi-module system with BiDFETs, custom passives

Year 2

Prototype B
208:480V, 3ϕ, 15kW
Paralleled Prototype A

- Gen 1 devices evaluated in *Prototype A*
- *Gen 2 to Foundry*

- Fe_4N magnetic core in *Prototype A*

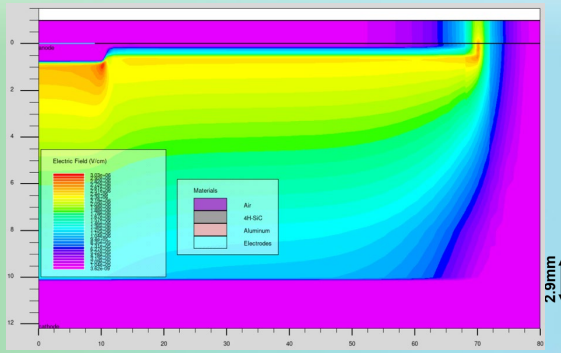
Year 1

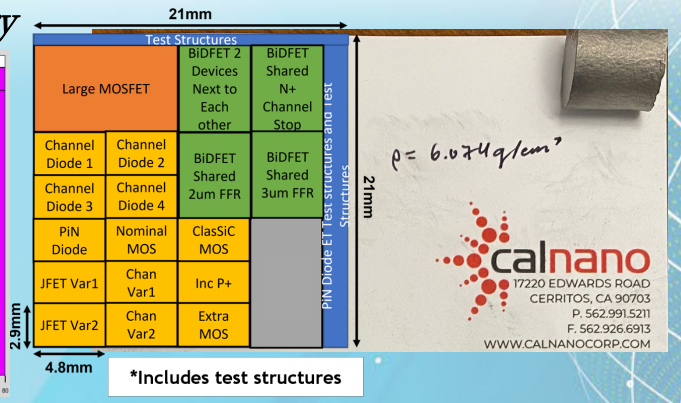
Prototype A
208:480V, 3ϕ, 3kW
Single SST Module

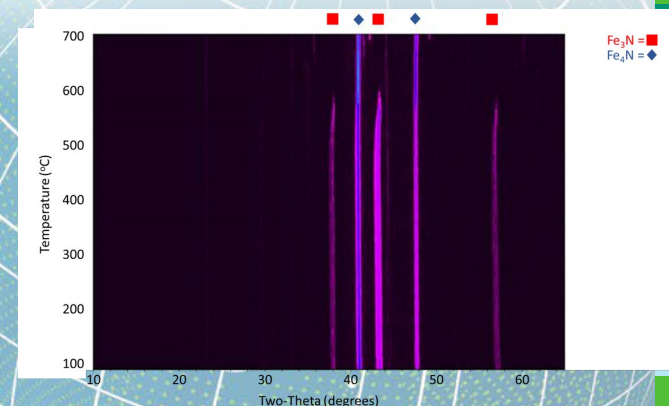
COTS devices with individual drain connected switches

- Process simulation and design
- Transfer process to SiC foundry
- *Gen 1 BiDFET to Foundry*

- Ball milling/powder purification Fe_4N powder at scale
- Production of Fe_4N Transformer Core

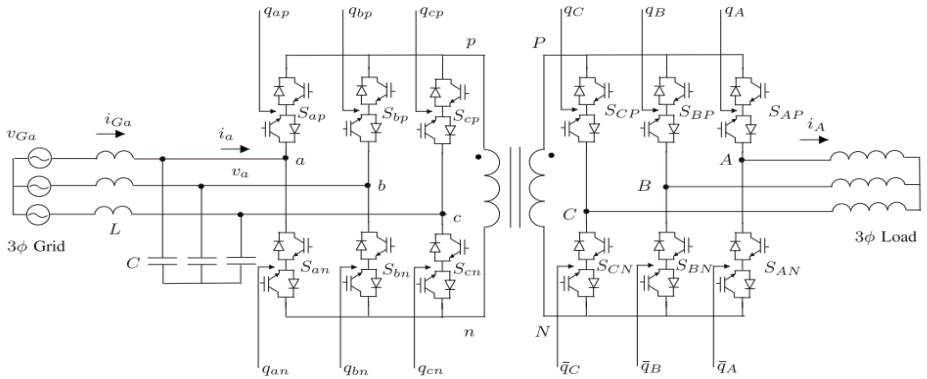






AC:AC DAB Circuit Development

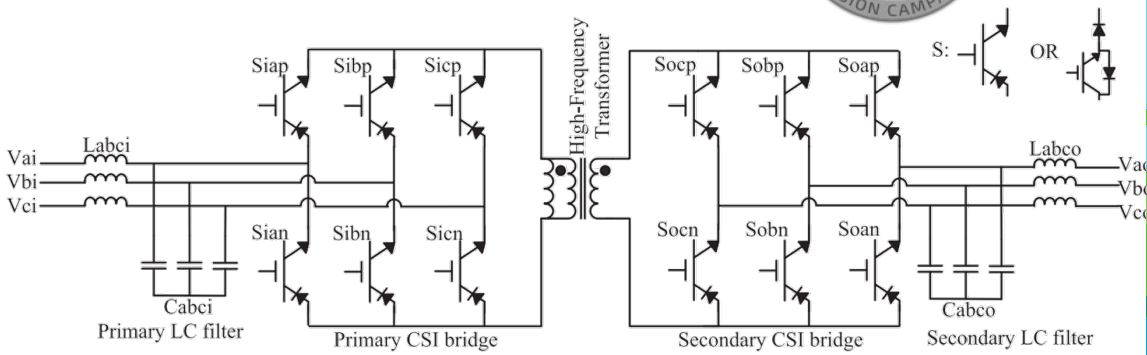
Isolated Indirect Matrix Converter



Basu K, Shahani A, Sahoo AK, Mohan N. A single-stage solid-state transformer for PWM AC drive with source-based commutation of leakage energy. IEEE Transactions on Power Electronics. 30(3):1734-46.

- 12 bidirectional switches
- Unidirectional power flow (circuit structure asymmetric)
- HF transformer acts as a pseudo DC link
- Load-side bridge operates at $2f_{switch}$ line-side bridge

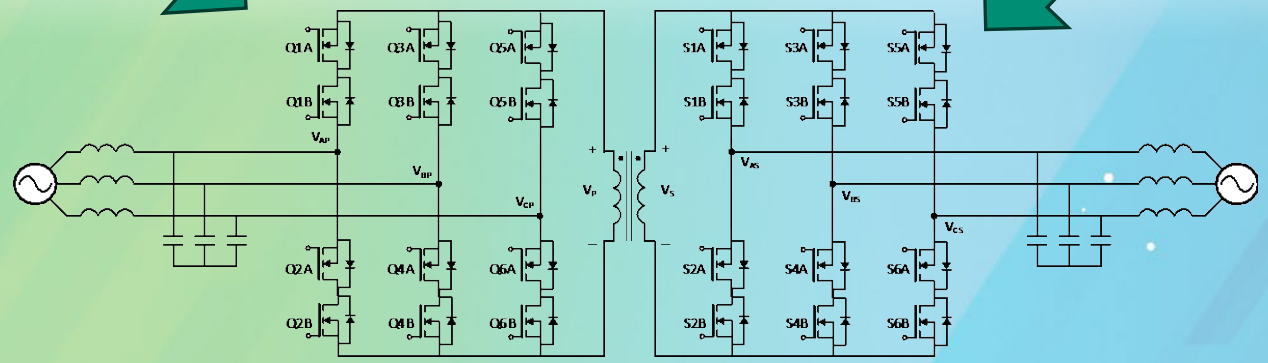
Dyna-C (GaTech)



Prasai A, Chen H, Divan D. Dyna-C: A topology for a bi-directional solid-state transformer. In APEC 2014 (pp. 1219-1226).

- 12 reverse-blocking switches (not 4-quadrant)
- Symmetric around the high-frequency transformer
- *Magnetizing Inductance* for stored energy
- *Unipolar* magnetizing current

AC:AC DAB



- 12 bidirectional switches
- *Bipolar* magnetizing current
- Symmetric around the HF transformer
- $2f_{Transformer} = f_{switching}$
- *Leakage Inductance* for stored energy
- Time varying phase shift for energy transfer
- L-L Filter Capacitors act as pseudo DC-link

AC:AC DAB Circuit Development

SST Modeling and Simulation

Derived Analytical Solution to Space Vector Modulation Approach

- Each bridge applies 2 switching states and a ∅-vector state to local winding
- Polarity of switching vectors alternates each switching period

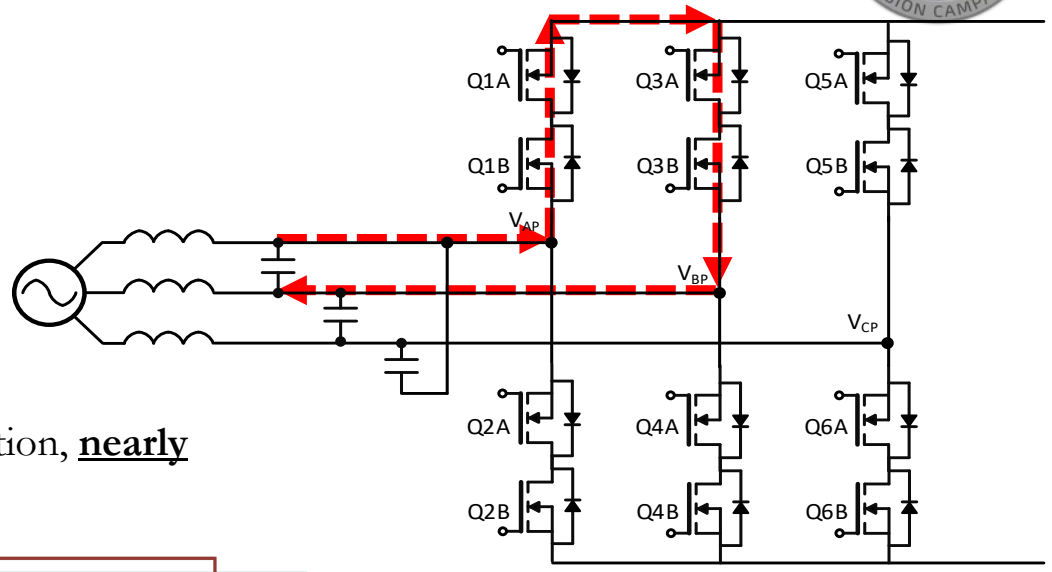
→ Produces bipolar 2-level transformer waveform at $\frac{1}{2} f_{switch}$

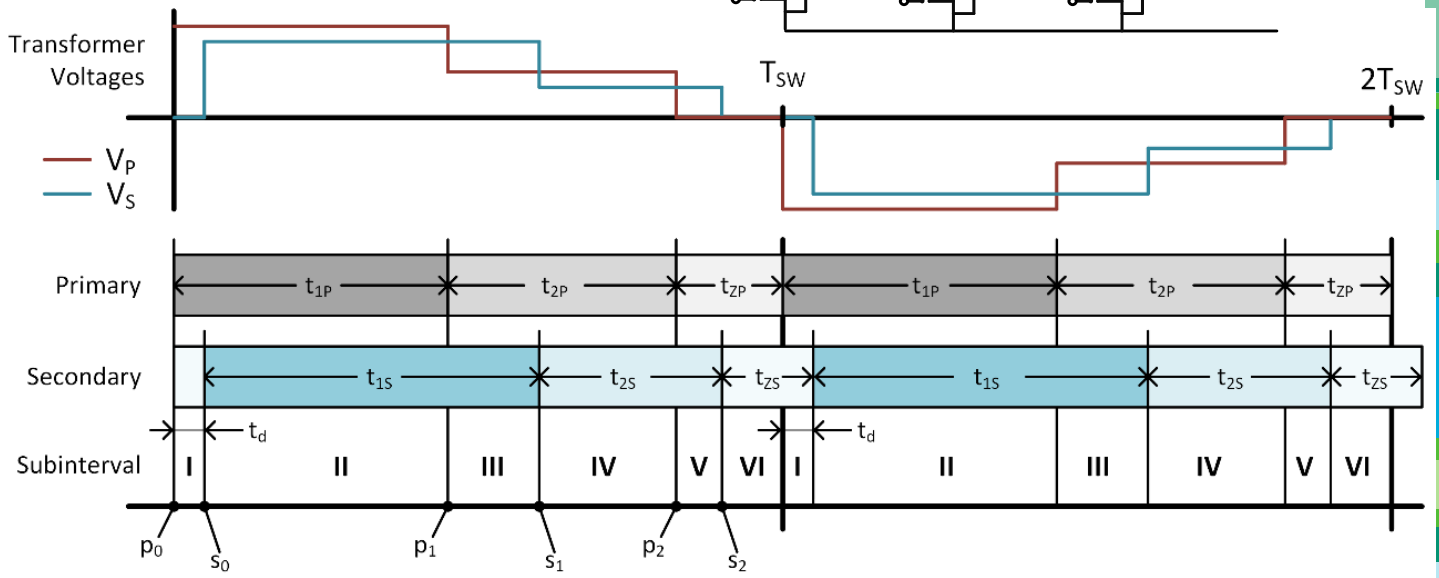
Furthermore, **the switching frequency must be the same** on primary and secondary side

However, besides these key parameters, which link primary and secondary operation, **nearly all other parameters are independent**.

Of particular interest to the capabilities of the SST:

- Primary **grid voltage magnitude**: $\Diamond(V_{LL,P} \neq V_{LL,S})$
- Primary **grid phase**: $\Diamond(\phi_P \neq \phi_S)$
- As a consequence the item above, primary **grid frequency**: $\Diamond(\omega_P \neq \omega_S)$
- As a consequence of all of the above, **reactive power exchange**: $\Diamond(Q_P \neq Q_S)$



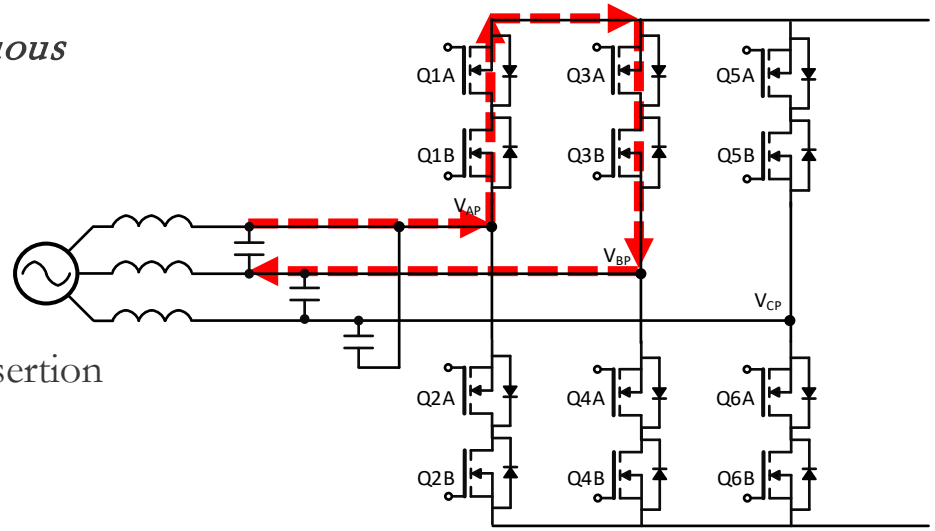


NB: Vector durations vary with the SVM reference angle → subinterval sequence of switching constantly changing → requires piecewise linear calculation of power transfer

AC:AC DAB Circuit Development

SST Modeling and Simulation

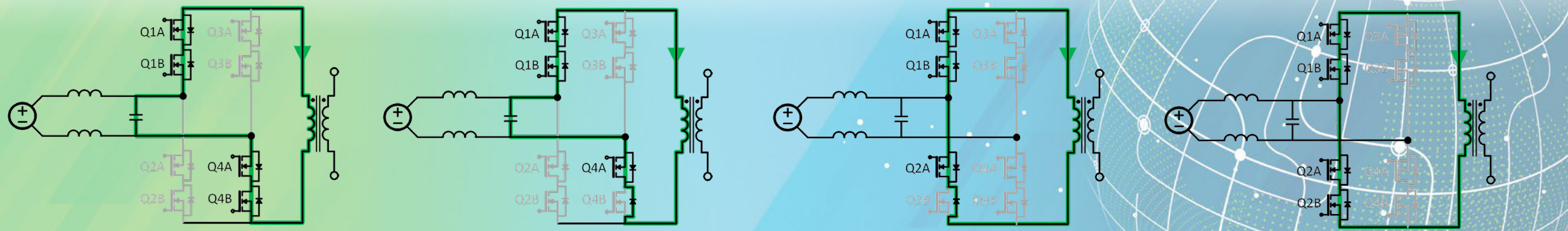
- **Adaptive Dead Time for Safe Commutation**
  - Risk of ***shoot-through faults*** exists due to line-line filter capacitor at switching node
  - Highly inductive transformer current contains significant energy; ***requires continuous conduction path*** to avoid destroying BIDFETs
    - 4-stage commutation known issue in Matrix converters
  - Sequence of switching actions is shown below for a simplified circuit
  - Appropriate delay generation depends on **polarity of transformer current;**
  - transformer current polarity detection must accurate to prevent erroneous delay insertion



For delay time T_d and primary current I_P:

If $I_P > 0$:
- QxA turn-off is delayed by T_d
- QxB turn-off is not delayed
- QxA turn-on is delayed by T_d
- QxB turn-on is delayed by $2T_d$

If $I_P < 0$:
- QxA turn-off is not delayed
- QxB turn-off is delayed by T_d
- QxA turn-on is delayed by $2T_d$
- QxB turn-on is delayed by T_d



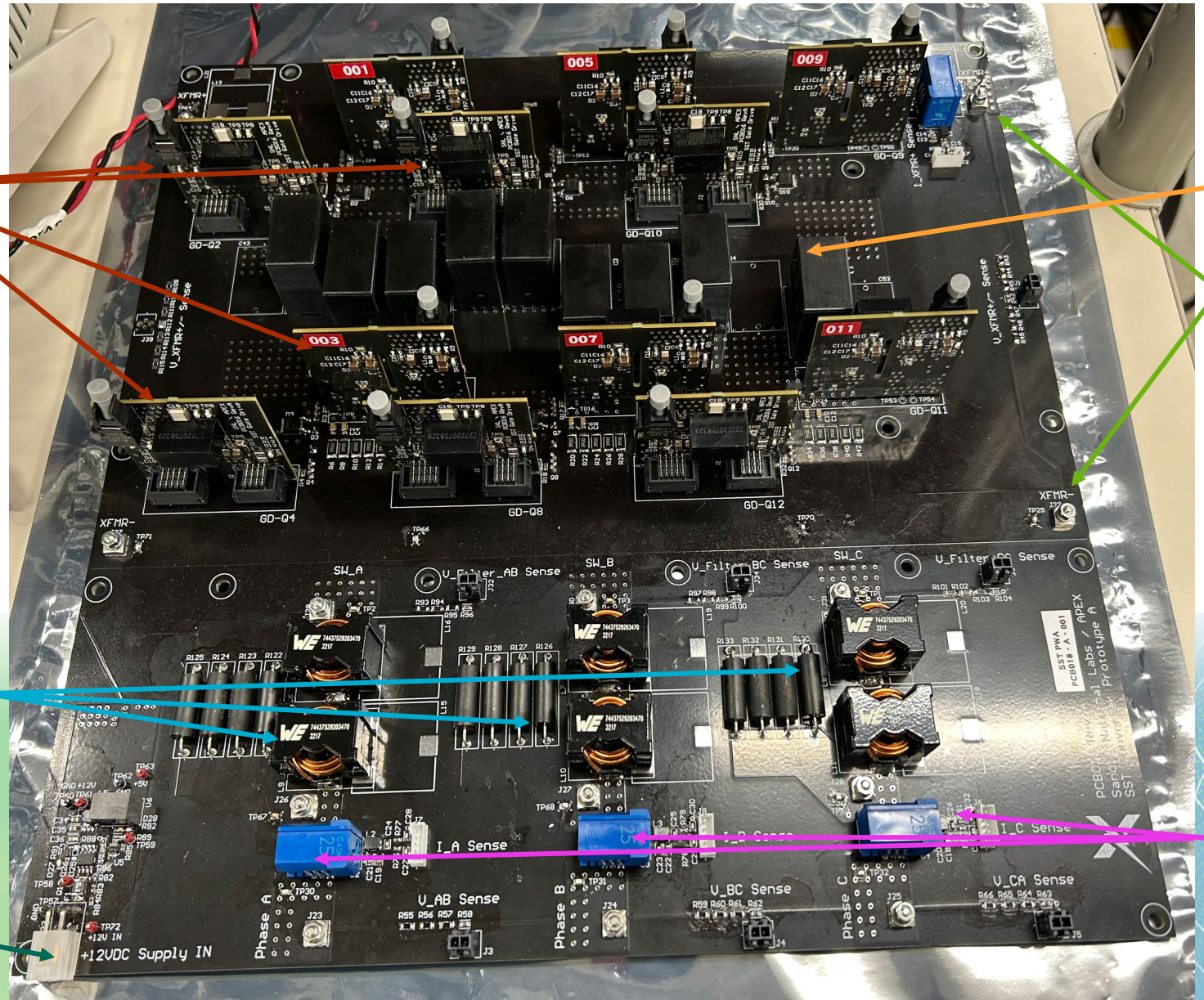
AC:AC DAB Circuit Development

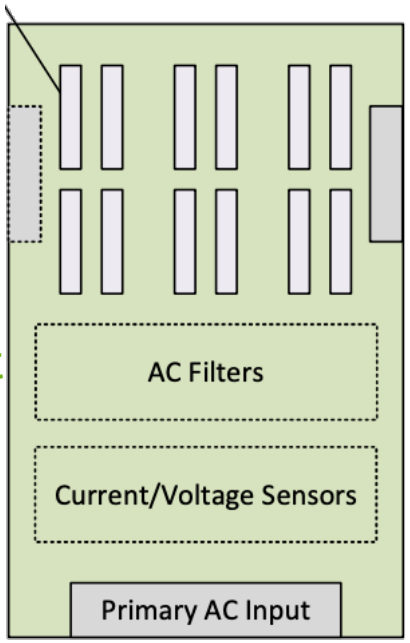
Circuit Build

Gate Driver Boards (optical drive)

Snubber Caps

Xformer Interconnect





Commercial "BiDFETs" (bottom side)

CLC Input/Output Filter ΦA,B,C

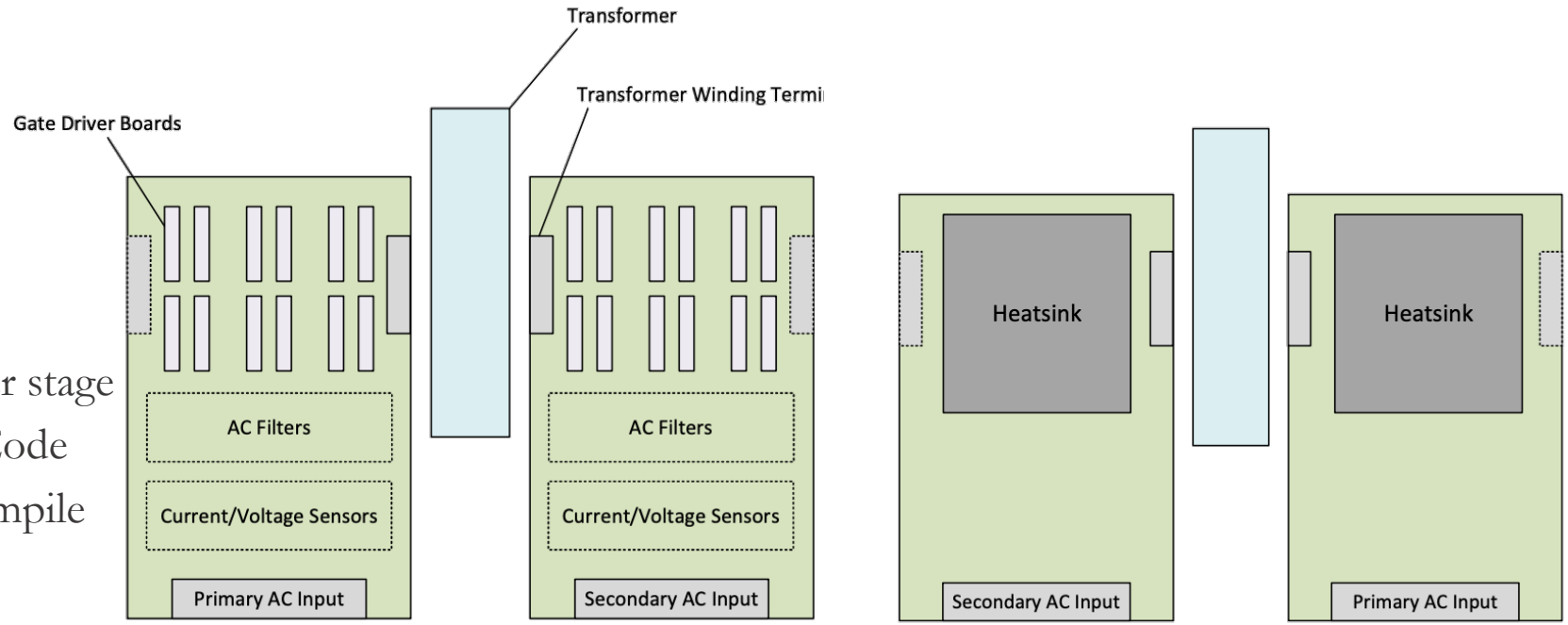
12V Aux Power

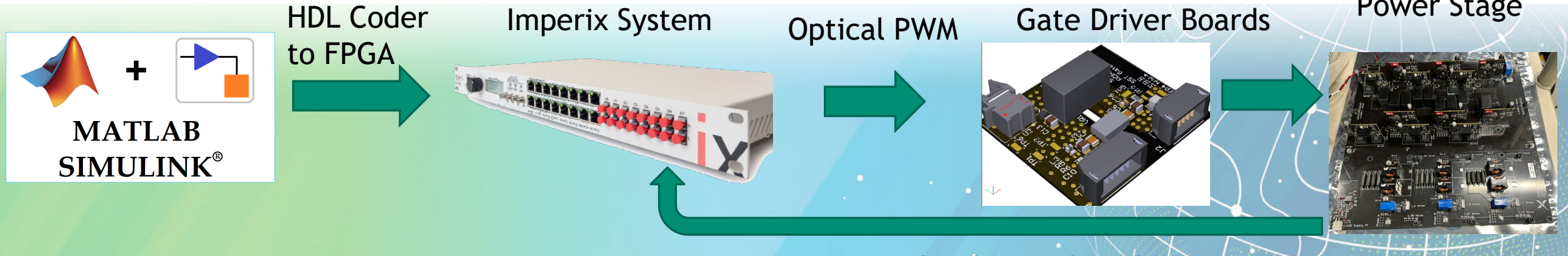
ΦA,B,C Current Measure

AC:AC DAB Circuit Development

Rapid Controls Prototyping

- **Controller Board**
  - Simulink control via Imperix FPGA
  - Faster validation of gate drive and power stage
  - PLECS simulation converted to HDL Code
  - Control system alteration without re-compile
  - f_{switch} = 50 kHz

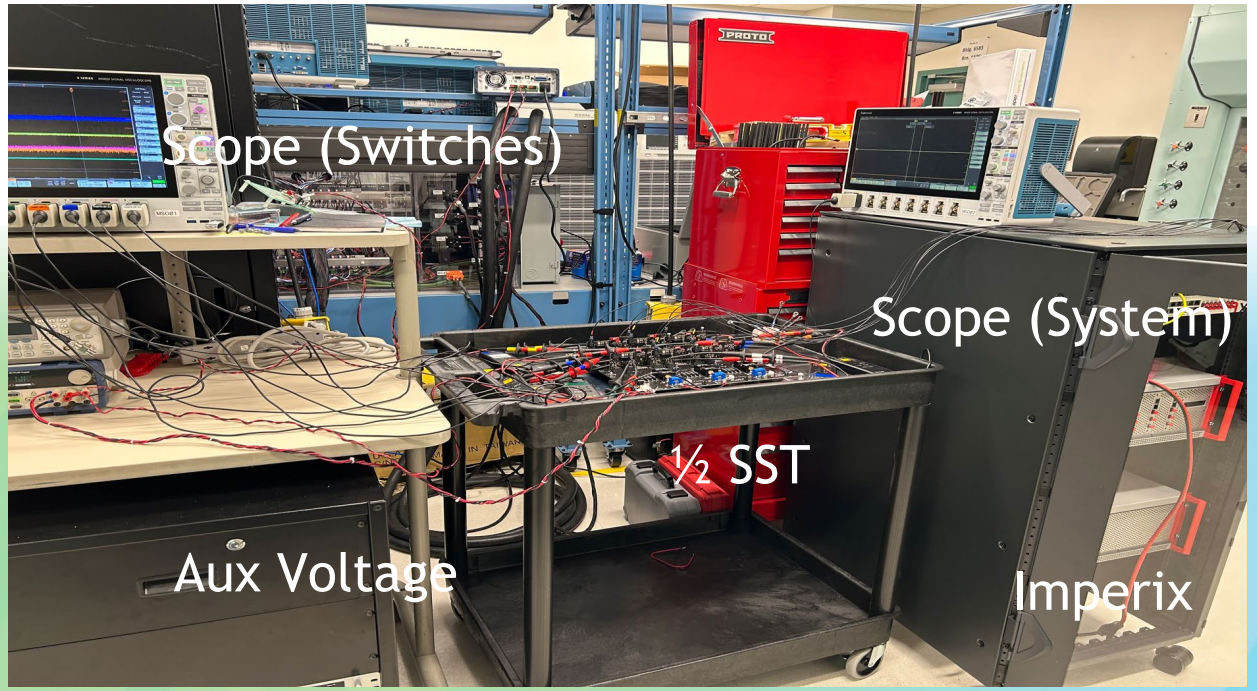


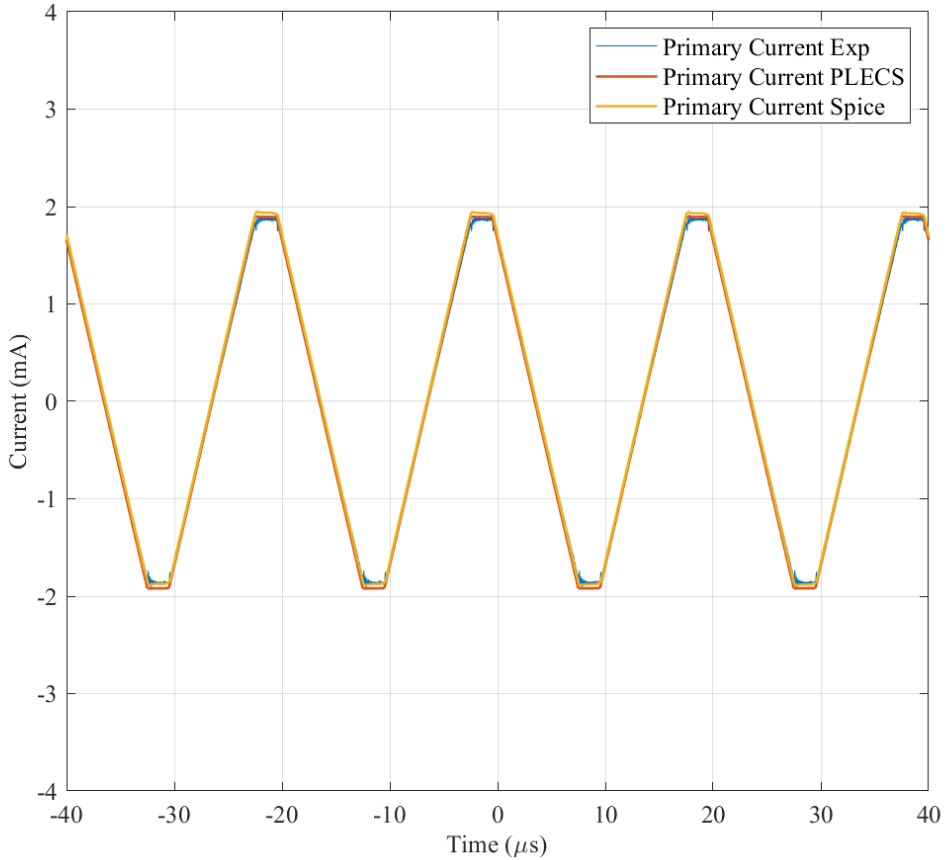


AC:AC DAB Circuit Development

Circuit Test

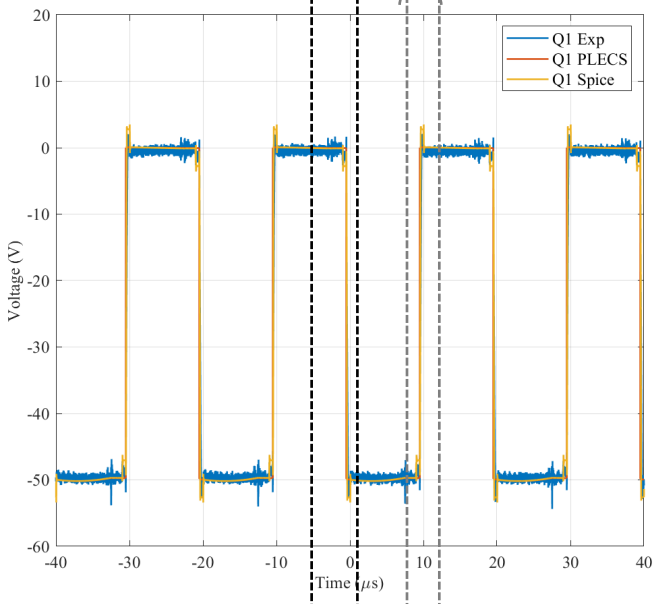
- Currently undergoing LV hardware testing
- So far, circuit works as expected
- Expected final current = 6.25 A
  - LV testing up to 1/3 final current levels

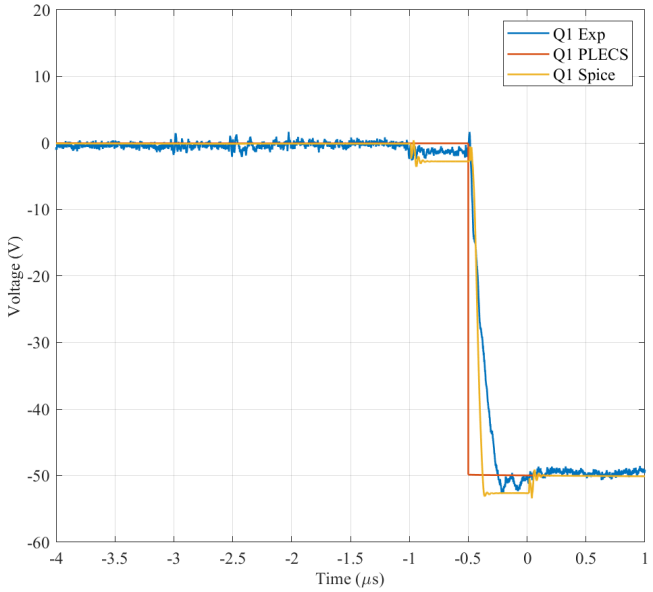


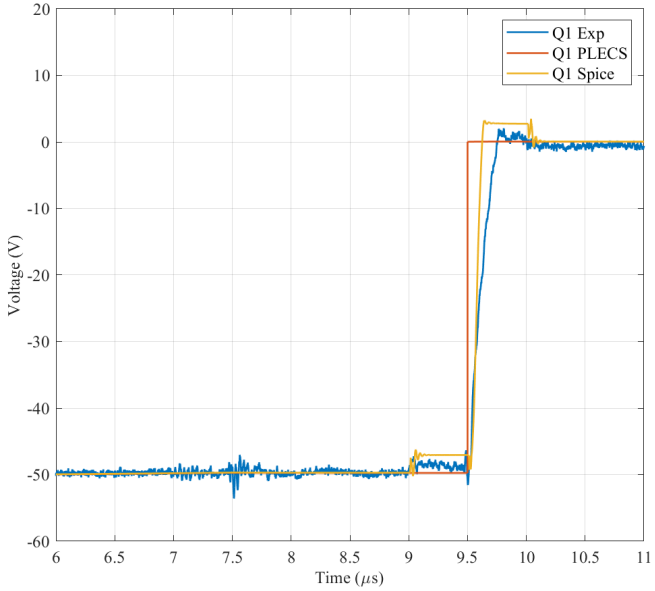


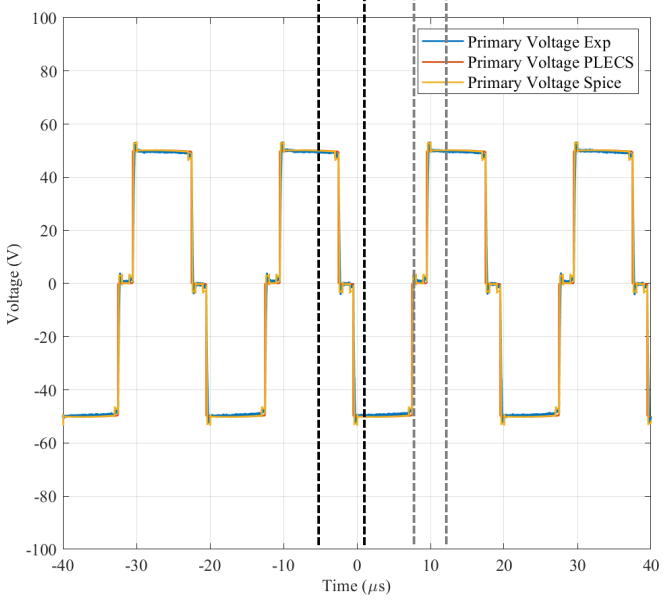
AC:AC DAB Circuit Development

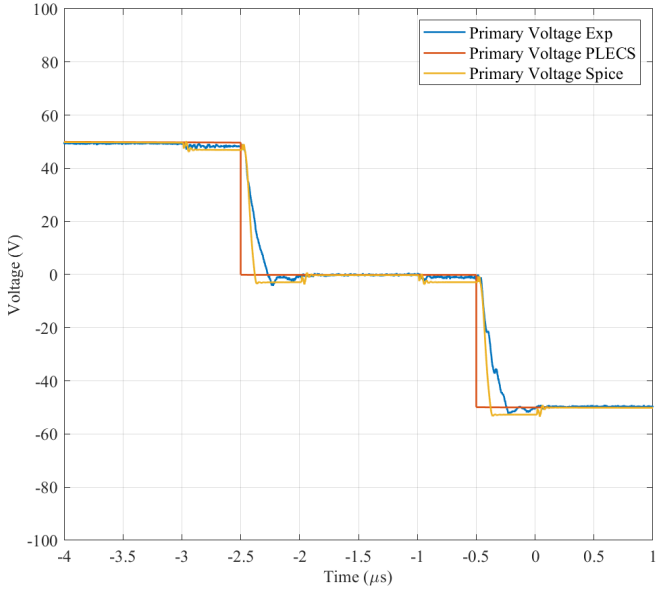
Circuit Test

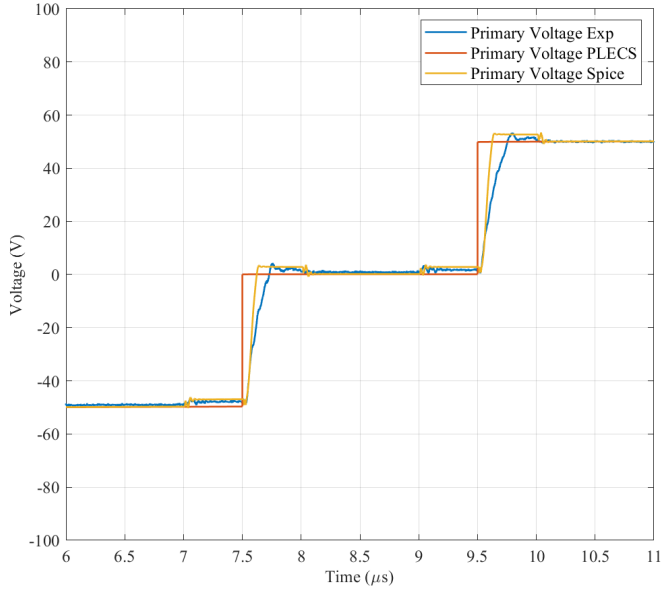








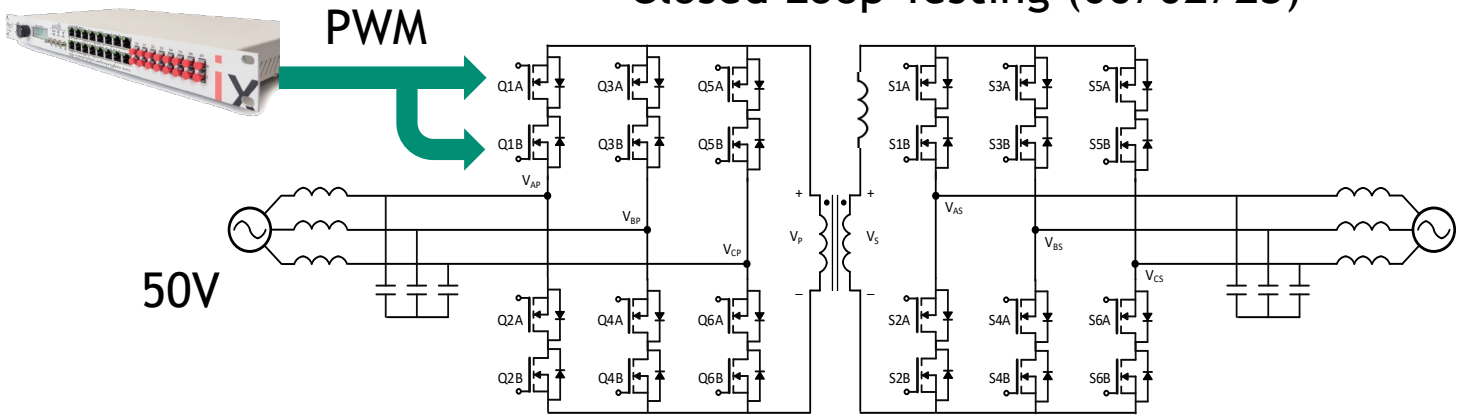




AC:AC DAB Circuit Development

Circuit Test

Closed Loop Testing (06/02/23)



Low Voltage Testing (50V)

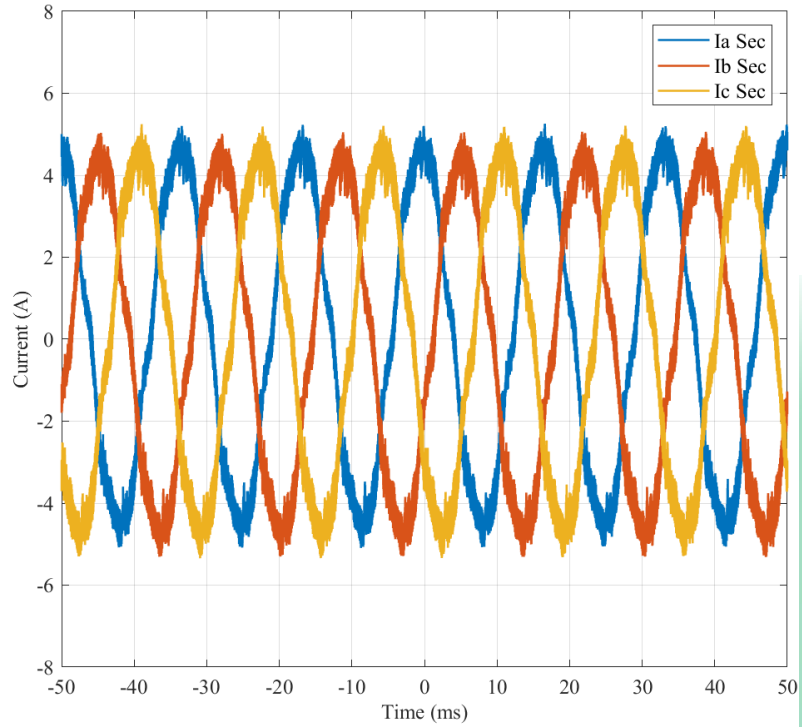
Power Transfer: 750W (40%)

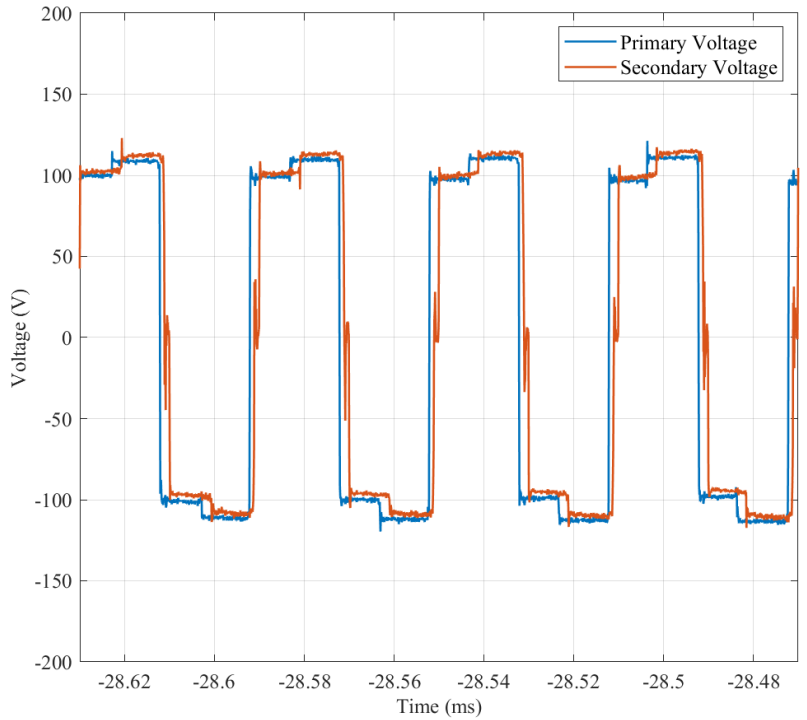
Average Efficiency: 95%

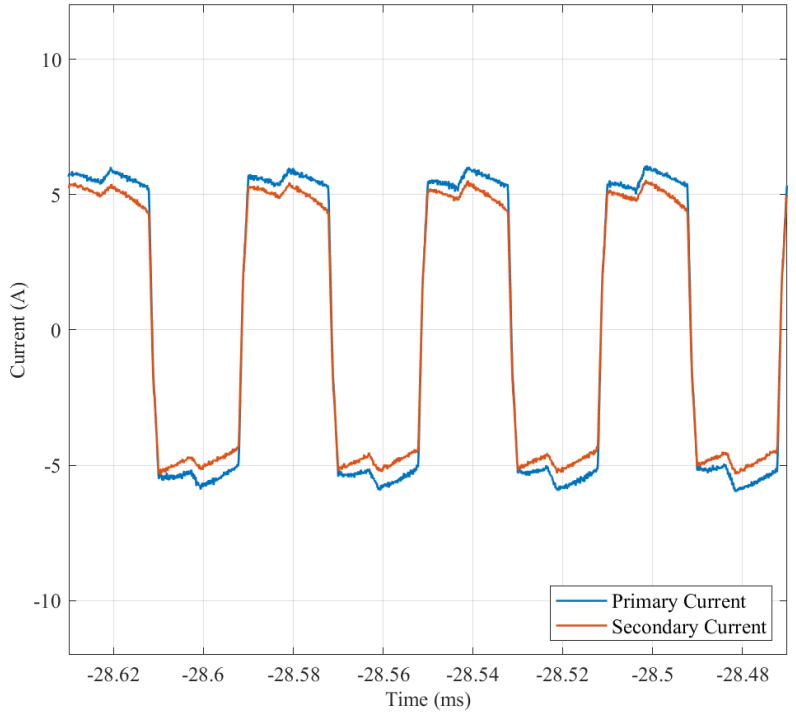
Open Loop: ✔

Closed loop P: ✔

Closed loop Q: ✔







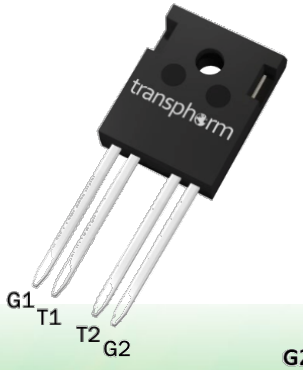
Future Work

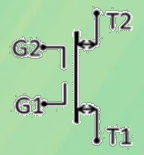
High Power and Grid Forming Mode Testing

Insertion of "Commercial" Four Quadrant GaN Switches

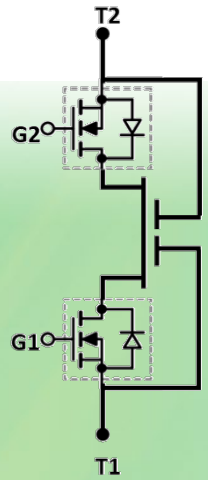
transphorm

TP65F060WS
TO-247-4
(top view)





FQS symbol



FQS schematic

Power Transfer: 750W (40%)

Average Efficiency: 95%

Open Loop: ✔

Closed loop P: ✔

Closed loop Q: ✔

$f_{in} \neq f_{out}$

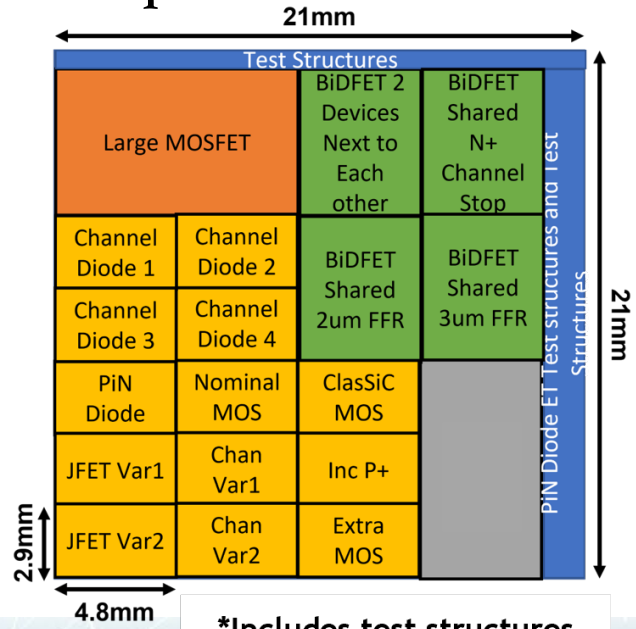
$Q_{in} \neq Q_{out}$

$V_{in} \neq V_{out}$

$\phi_{in} \neq \phi_{out}$

Closed loop V (Grid Forming)

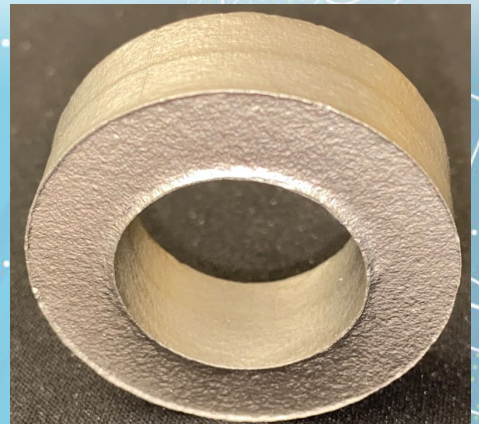
1st As-designed SiC BiDFET lot September 2023



*Includes test structures

1st SPS Fe_4N Transformer Core Sept. 2023

OD 4.18cm, ID 2.62cm, and HT 1.25 cm



Thank you

Jack Flicker

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