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Photovoltaic Microinverter Testbed for Multiple Device Interoperability

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Abstract

IEEE Standard 1547-2003 [1] conformance of several interconnected microinverters was performed by Sandia National Laboratories (SNL) to determine if there were emergent adverse behaviors of co-located aggregated distributed energy resources. Experiments demonstrated the certification tests could be expanded for multi-manufacturer microinverter interoperability. Evaluations determined the microinverters' response to abnormal conditions in voltage and frequency, interruption in grid service, and cumulative power quality. No issues were identified to be caused by the interconnection of multiple devices.

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NOMENCLATURE

DOE	Department of Energy
SNL	Sandia National Laboratories
IEEE	Institute of Electrical and Electronics Engineers
NEC	National Electric Code
PV	Photovoltaic
DC	Direct Current
BOS	Balance of Systems
AC	Alternating Current
W	Watts
STC	Standard Test Conditions
VOC	Open-Circuit Voltage
ISC	Short-Circuit Current
V	Volts
PCC	Point of Common Coupling
R	Resistive
L	Inductive
C	Capacitive
CT	Current Transducer
s	Seconds
Hz	Hertz
RLC	Resistive/Inductive/Capacitive
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
VAr	Volt-Ampere Reactive

1. INTRODUCTION

The use of microinverters in residential photovoltaic (PV) systems has increased to become a significant player in the market [2]. This is due to several favorable attributes inherent to the microinverter topology. These attributes include the mitigation of direct current (DC) balance of system (BOS) requirements, eliminating the presence of high DC voltage, reducing exposure to DC voltage (favorable for new NEC 690.12 rapid shutdown requirements [3]), and the reduction of the impact that module mismatch and shading has on the power generation of a PV system. While these attributes can have a significant positive impact, mass implementation can only be possible if sufficient interoperability of interconnected microinverters can be achieved.

IEEE 1547 compliance, as well as UL 1741 [4], is achieved through individual testing of devices using IEEE Standard 1547.1-2005 [5] test procedures. Microinverters are designed to connect to one, sometimes two, individual PV modules, and therefore are most likely to be interconnected with many others in a PV array. Also, in a residential setting with more than one customer PV system connected to a service transformer, microinverters may be forced to function within short electrical distance from other microinverters of different manufacture. The testing herein addresses the concern of verifying listed microinverter compliance in such settings.

SNL ran IEEE 1547.1 conformance tests on a multi-manufacturer testbed of several interconnected microinverters. The purposes of the experiment were to:

- 1) Implement a method for evaluating interoperability of multiple interconnected microinverters.
- 2) Identify any interoperability issues caused by the interconnection of multiple devices.

Grid compatibility evaluations determined the voltage and frequency operating ranges, the inverter's response to a voltage/frequency sag or swell, and the response to an interruption in grid service. Test criteria are specified in IEEE 1547.1.

1.1. Test Setup

The tests were performed using PV power from a testbed of 21 monocrystalline, 60 cell modules. The modules were arranged in three horizontal rows of seven modules in landscape orientation, mounted on a fixed, latitude-tilt rack (35°). The modules were rated 245 W_P at standard test conditions (STC), resulting in three rows of approximately 1.7 kW_{DC} each, or approximately 5.1 kW_{DC} total for the entire array.

Each module in a row was connected to a microinverter in a string of 7 paralleled, identical microinverters, with a different manufacturer of microinverter used on each string. Each of the three microinverter models chosen was compatible with the module characteristics, including input power range, maximum open-circuit voltage (VOC), peak power tracking voltage, and maximum short-circuit current (ISC).

Each microinverter model had a 240 V_{AC} nominal output with two models providing two 120 V_{AC} lines referenced to neutral and one model providing a 240 V_{AC} line-to-line output with no neutral. The three strings of microinverters under test were connected to a point of common coupling (PCC) on the secondary side of the service transformer, as three residential systems might be in the field, but with much greater electrical proximity in this case. The total system rated AC power was approximately 4836 W_{AC}. A one-line diagram of the testbed configuration is shown in Figure 1.

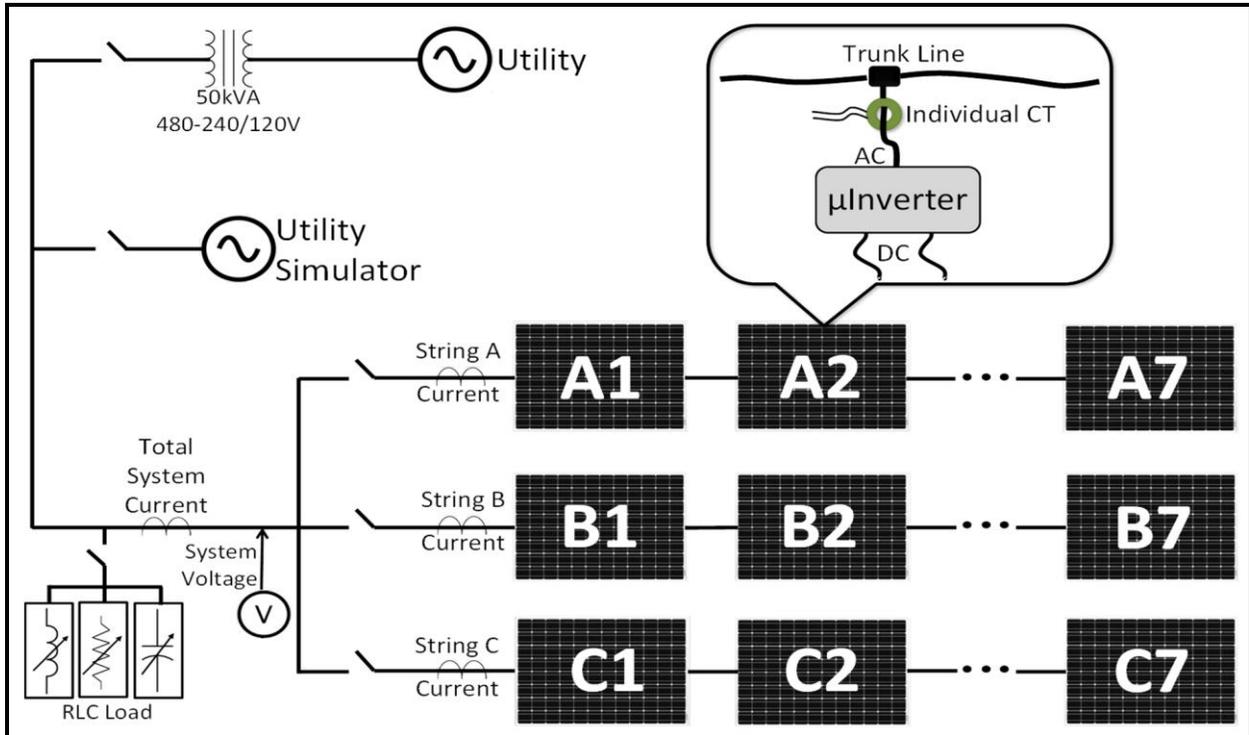


Figure 1. Microinverter testbed configuration diagram.

The testbed was set up with the ability to disconnect each string individually for different configurations. The grid and transformer could be switched in and out with an AC disconnect for normal operation and anti-islanding tests. The Grid Simulator could be connected in lieu of the utility for grid compatibility tests. The Grid Simulator had regenerative capability for the testbed power output. Configurable resistive (R), inductive (L), and reactive (C) loads could be interconnected for anti-islanding testing.

Instrumentation was installed, calibrated, and configured to collect the many parameters needed for test results. Wide-band current transducers (CTs) were installed on one leg of each microinverter to monitor individual AC current outputs and harmonics. CTs were also installed to monitor each string and total system level current and harmonics. The average of the CT calibration errors for the entire system was 0.7%. No DC instrumentation was installed.

A single system voltage probe was installed at the PCC to monitor system voltage, frequency, and voltage harmonics pertaining to the entire paralleled system. The PCC voltage measurement instrument was calibrated to no greater than 0.07% error for the range of voltages tested. Other instrumentation was installed, including irradiance measurements, ambient temperature, module temperatures, and trigger signals from the simulator and grid AC disconnect.

The approach to the testing and analysis was intended to bring to light any issues caused by the interconnection of several microinverters. This was done by performing the tests at the system-level (all 21 units interconnected), then the string-level (only one string of 7 units of the same manufacturer interconnected), and finally at the individual-level (just one unit interconnected). The approach allowed for investigation of discrepancies between levels, wherever necessary.

2. INTERCONNECTION TESTS AND RESULTS

Selected type tests were performed on a testbed of microinverters from three different manufacturers to demonstrate that the interconnection functions and equipment of the microinverters could be tested to IEEE 1547.1 when interconnected with other units and to reveal any adverse behaviors caused by multi-manufacturer microinverter interconnection. The tests were modified to apply to the testing of several interconnected microinverters, with instrumentation to provide results as a system as well as each individual unit.

Each test was repeated a minimum of 3 times. Due to the 21 individual sets of AC parameters collected, string level data were plotted in many cases for visual purposes. It is important to note that individual currents were also examined in all cases. The small residual current levels seen after the microinverters stopped producing power were due to filtering elements within the devices.

The voltage and frequency trip time tests were only performed on the entire system and not on each string individually, nor any pairs of strings. The over- and undervoltage magnitude tests were performed at the system level, each string, and select individual units. The data collection resolution for the magnitude tests was one data point per second. The data collection resolution for the trip time tests was six thousand data points per second.

2.1. Test for response to abnormal voltage conditions

The tests for response to abnormal voltage conditions are specified in IEEE 1547.1, Section 5.2. The tests determined the magnitude and trip time for the specified tests. Each procedure was applied to the testbed as an interconnected system using the Grid Simulator, and subsequent string and individual level tests were performed as needed. All result voltages displayed pertain to each microinverter's specific voltage level by estimating the voltage rise to each along the string, taking into account the conductor segment lengths, impedances, and currents in each segment. The power output of the units varied with outdoor conditions but was not critical to the tests, although clear sky conditions were sought.

2.1.1. Test for overvoltage – magnitude (>110%)

For the overvoltage magnitude test, a function was executed through the Grid Simulator to ramp the voltage up to 112.5% (270 V on a 240 V base) and observe the trip voltage magnitude of each unit, repeated 4 times. A conservative slope of 0.1 V/s was used to accommodate all manufacturer measurement accuracies and detection times [5]. Figure 2 shows a plot of the ramp function executed by the Grid Simulator.

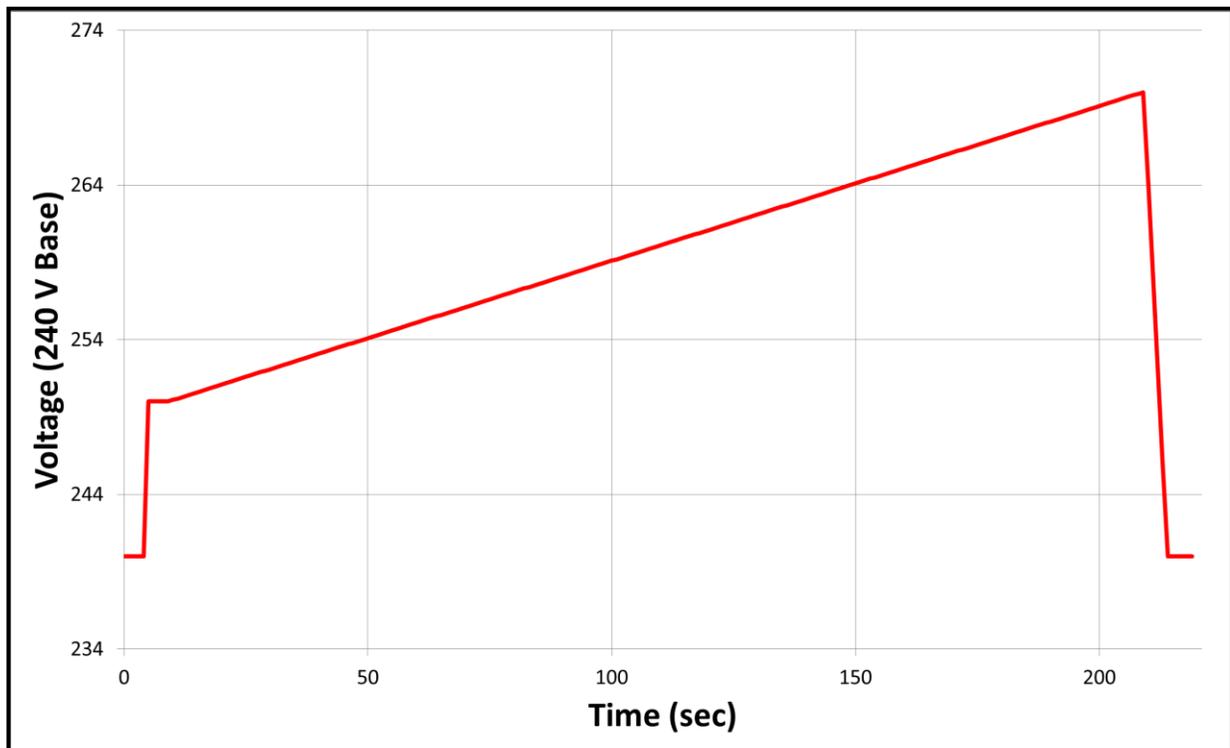


Figure 2. Overvoltage ramp function.

During the system and string level tests all units tripped off before the execution of the entire voltage function. One unit from each manufacturer that was found to consistently produce power closest to the expected trip voltage was chosen to be tested individually.

Table 1 shows each unit's 4-test average trip voltage and standard deviation for the system and string level tests, as well as individual level averages for those chosen for individual tests.

Table 1. Average trip voltages, overvoltage tests (110%/264 V).

Unit	Expected Trip Voltage	Overvoltage 4-Test Averages and Standard Deviations					
		System		String		Individual	
		Voltage	Std Dev	Voltage	Std Dev	Voltage	Std Dev
A1	270.6	264.7	0.1	264.6	0.5	264.9	0.1
A2	270.6	263.0	0.1	263.1	0.1		
A3	270.6	263.9	0.0	264.1	0.3		
A4	270.6	263.7	0.2	263.7	0.3		
A5	270.6	264.3	0.1	264.2	0.3		
A6	270.6	262.4	0.1	262.5	0.1		
A7	270.6	263.6	0.1	263.8	0.4		
B1	270.6	265.0	0.1	267.3	0.1		
B2	270.6	264.7	0.1	266.6	0.1		
B3	270.6	266.3	0.1	268.9	0.1		
B4	270.6	266.9	0.4	269.1	0.1		
B5	270.6	266.8	0.1	269.1	0.2		
B6	270.6	268.2	0.2	270.4	0.9	268.3	0.1
B7	270.6	267.1	0.1	269.6	0.7		
C1	269.1	265.5	0.1	265.4	0.4	265.1	0.5
C2	269.1	265.0	0.2	264.8	0.4		
C3	269.1	262.2	0.3	262.3	0.3		
C4	269.1	261.5	0.2	262.0	0.1		
C5	269.1	260.6	0.5	261.4	0.1		
C6	269.1	261.8	0.2	261.8	0.4		
C7	269.1	261.7	0.4	262.1	0.4		

¹Expected trip voltage was calculated to estimate the worst case trip voltage expected considering each model's measurement accuracy at the test voltage level.

Table 1 shows that there were not any differences between the test levels (system, string and individual) significant enough to suspect any issues caused by the interconnection of multiple devices. Furthermore, the standard deviations of the repeated test values of each unit show the consistency of behavior of the units within each test setting. The observed generation beyond the standard threshold was due to the measurement accuracies of the microinverters.

2.1.2. Test for overvoltage – Trip time (>110% and ≥120%)

For the overvoltage trip time tests, a function was executed through the Grid Simulator to step the voltage up to 112.5% (270 V on a 240 V base) and 125% (300 V on a 240 V base) to observe the trip time of each unit for each overvoltage level, repeated 4 times. The standard trip time limits are 60cycles/1.00s for voltages >110%/264V but <120%/288V, and 10cycles/0.16s for voltages ≥120%/288V [1]. Figure 3 and Figure 4 show the respective waveform plots of the individual string currents and voltage for each overvoltage trip time test. No generation beyond the standard trip time thresholds was observed. Manufacturers utilizing the majority of the allotted trip durations would ride through short voltage anomalies better and would be more immune to nuisance trips.

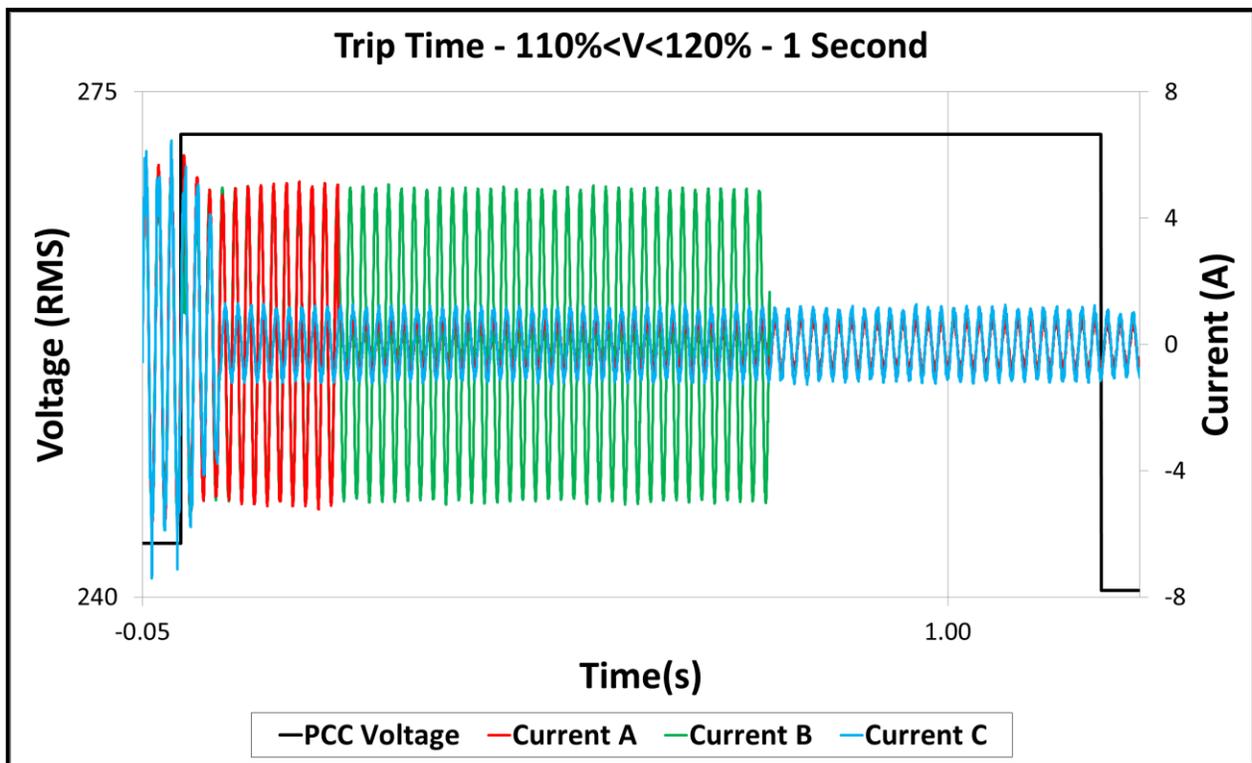


Figure 3. Overvoltage trip time test results, 112.5%.

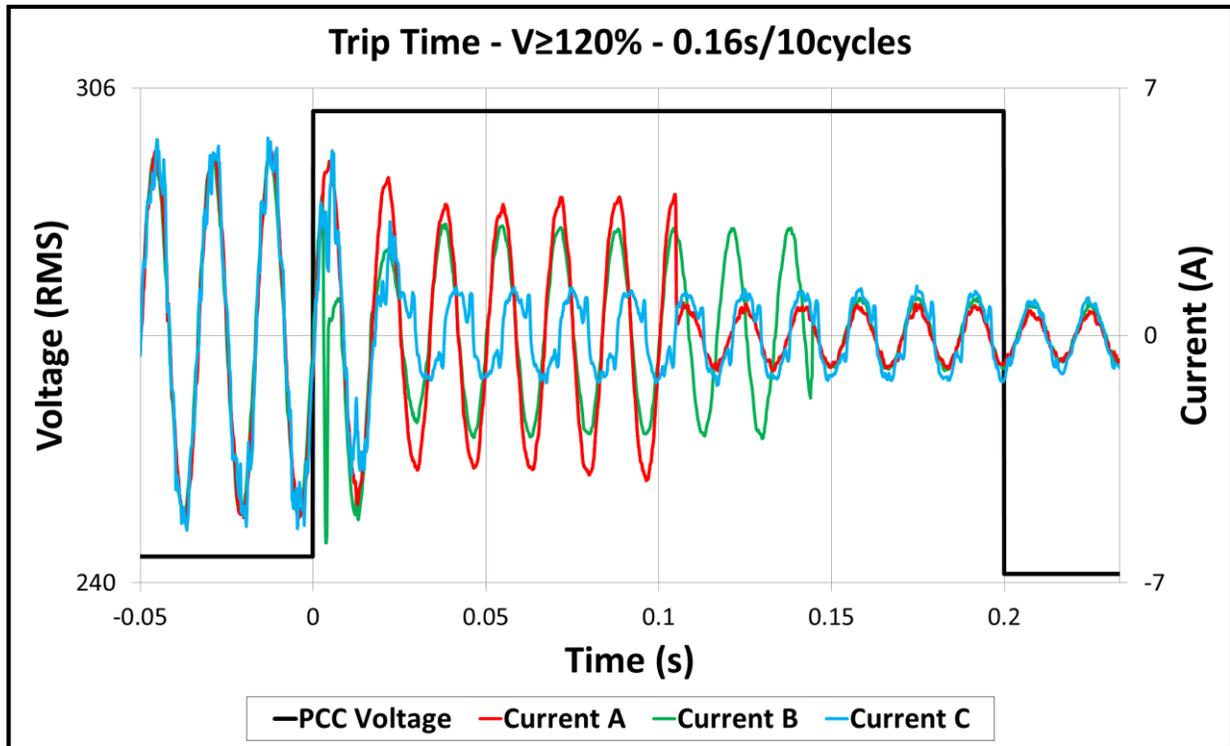


Figure 4. Overvoltage trip time test results, 125%.

2.1.3. Test for undervoltage - magnitude (<88%)

For the undervoltage magnitude test, a function was executed through the Grid Simulator to ramp the voltage down to 85% (204 V on a 240 V base) and observe the trip voltage magnitude of each unit, repeated 4 times. A conservative slope of 0.1 V/s was used to accommodate all manufacturer measurement accuracies and detection times [5]. Figure 5 shows a plot of the ramp function executed by the Grid Simulator.

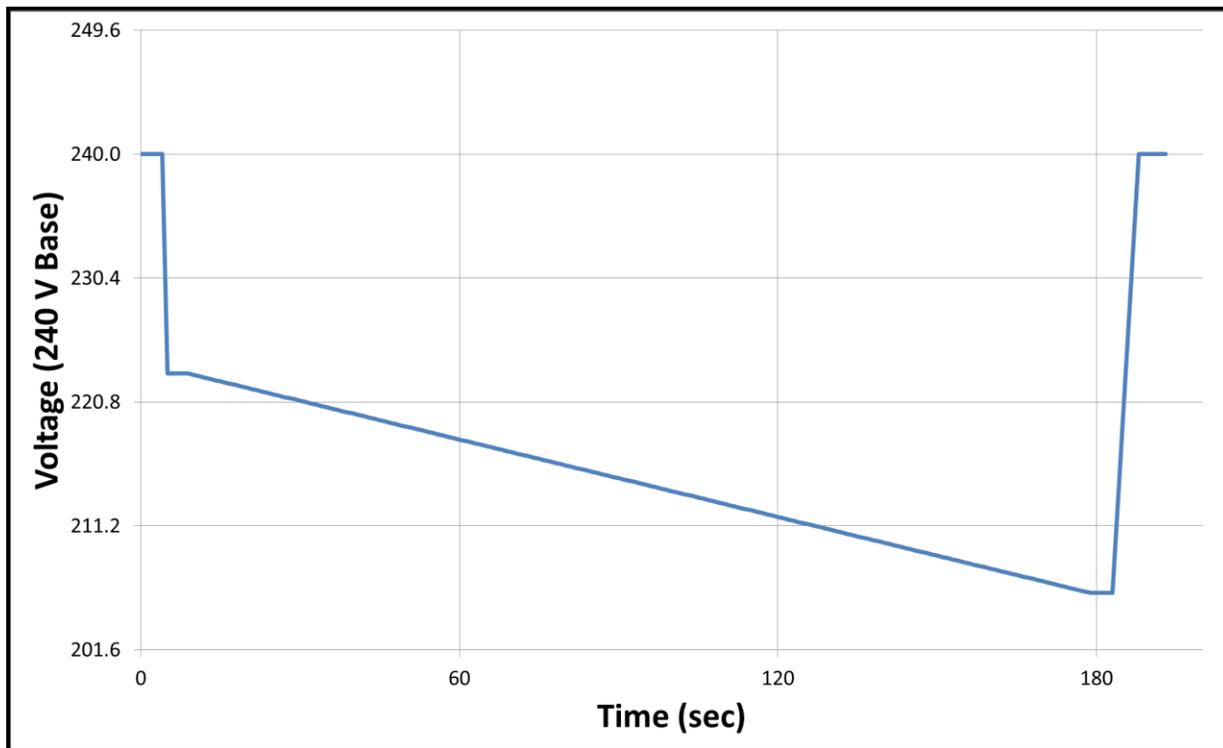


Figure 5. Undervoltage ramp function.

During the system and string level tests all units tripped off before the execution of the entire voltage function. One unit each from manufacturers A and B that were found to consistently produce power closest to the expected trip voltage were chosen to be tested individually.

Table 2 shows each unit's 4-test average trip voltage and standard deviation for the system and string level tests, as well as individual level averages for those chosen for individual tests.

Table 2. Average trip voltages, undervoltage tests (88%/211.2 V).

Unit	Expected Trip Voltage ¹	Undervoltage 4-Test Averages and Standard Deviations					
		System		String		Individual	
		Voltage	Std Dev	Voltage	Std Dev	Voltage	Std Dev
A1	202.8	213.2	0.2	213.3	0.1		
A2	202.8	212.5	0.5	212.4	0.3		
A3	202.8	212.2	0.2	212.3	0.2		
A4	202.8	213.1	0.9	212.7	0.2		
A5	202.8	211.6	0.3	211.7	0.4		
A6	202.8	213.0	0.5	213.2	0.5		
A7	202.8	210.8	0.2	211.1	0.2	210.9	0.1
B1	205.9	209.8	0.4	210.3	0.1	210.2	0.1
B2	205.9	210.0	0.5	210.1	0.3		
B3	205.9	211.2	0.2	211.6	0.2		
B4	205.9	211.7	0.4	212.0	0.0		
B5	205.9	211.3	0.2	211.2	0.3		
B6	205.9	212.3	0.2	212.5	0.1		
B7	205.9	211.4	0.3	211.6	0.2		
C1	207.3	219.0	0.6	218.8	0.3		
C2	207.3	218.0	0.3	217.7	0.1		
C3	207.3	216.0	0.4	215.7	0.1		
C4	207.3	215.9	0.3	215.8	0.1		
C5	207.3	216.0	0.3	215.9	0.1		
C6	207.3	216.0	0.1	215.9	0.2		
C7	207.3	216.1	0.2	216.0	0.1		

¹Expected trip voltage was calculated to estimate the worst case trip voltage expected considering each model's measurement accuracy at the test voltage level.

Table 2 shows that there were not any differences between the test levels (system, string, and individual) significant enough to suspect any issues caused by the interconnection of multiple devices. Furthermore, the standard deviations of the repeated test values of each unit again show the consistency of behavior of the units within each test setting. The observed generation beyond the standard threshold was due to the measurement accuracies of the microinverters.

2.1.4. Test for undervoltage – Trip time (<88% and <50%)

For the undervoltage trip time tests, a function was executed through the Grid Simulator to step the voltage down to 85% (204 V on a 240 V base) and 45% (108 V on a 240 V base) to observe the trip time of each unit for each undervoltage level, repeated 4 times. The standard trip time limits are 120cycles/2.00s for voltages <88%/211.2V, and 10cycles/0.16s for voltages <50%/120V [1]. Figure 6 and Figure 7 show the respective waveform plots of the individual string currents and voltage for each undervoltage trip time test. No generation beyond the standard trip time thresholds was observed.

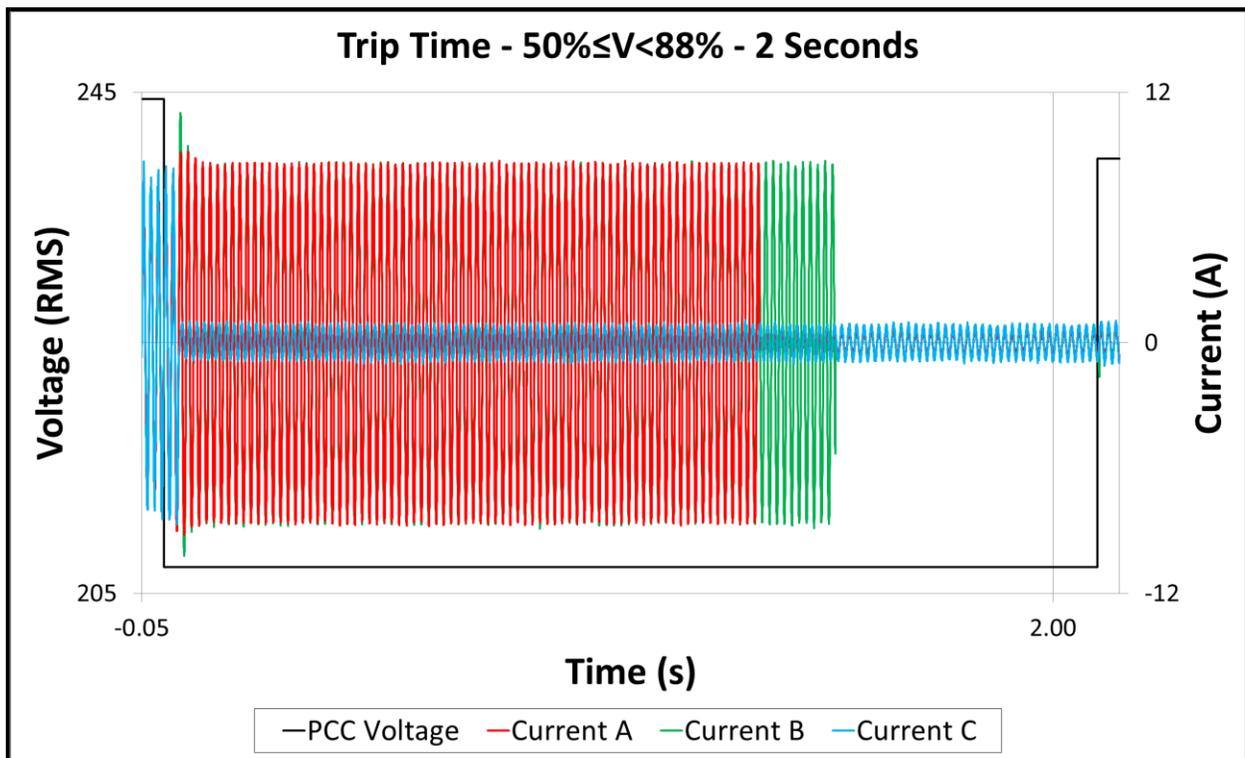


Figure 6. Undervoltage trip time test results, 85%.

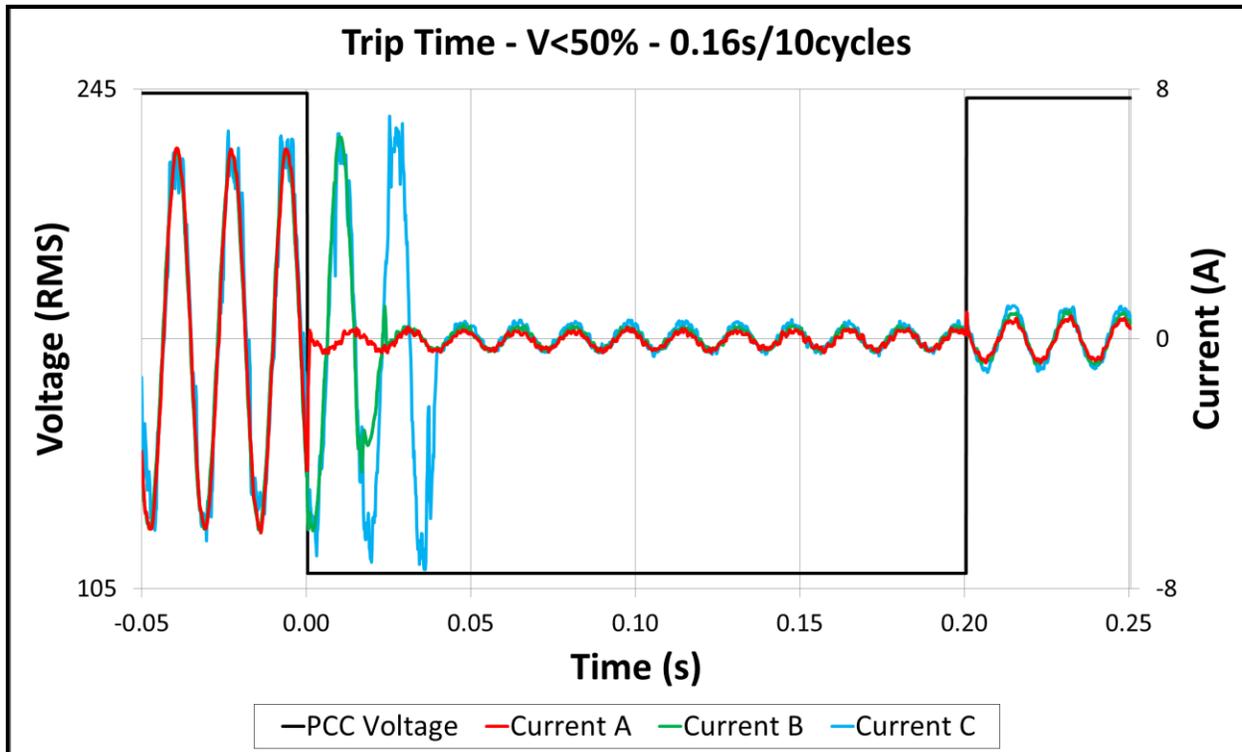


Figure 7. Undervoltage trip time test results, 45%.

2.2. Response to abnormal frequency conditions

The tests for response to abnormal frequency conditions are specified in IEEE 1547.1, Section 5.3. The tests determined the magnitude and trip time of each unit for the specified tests. Each procedure was applied to the testbed as an interconnected system using the Grid Simulator. The tests determined the magnitude and trip time for each condition function. Each procedure was applied to the testbed as an interconnected system using the Grid Simulator. The power output of the units varied with outdoor conditions but was not critical to the tests, although clear sky conditions were sought.

2.2.1. Test for overfrequency – magnitude (>60.5 Hz)

For the overfrequency magnitude test, a function was executed through the Grid Simulator to ramp the frequency up to 60.6 Hz as measured on the PCC voltage and observe the trip frequency magnitude of each unit, repeated 4 times. Figure 8 shows a plot of the individual microinverter real power outputs versus the increasing PCC frequency. All units tripped below the 60.6 Hz threshold.

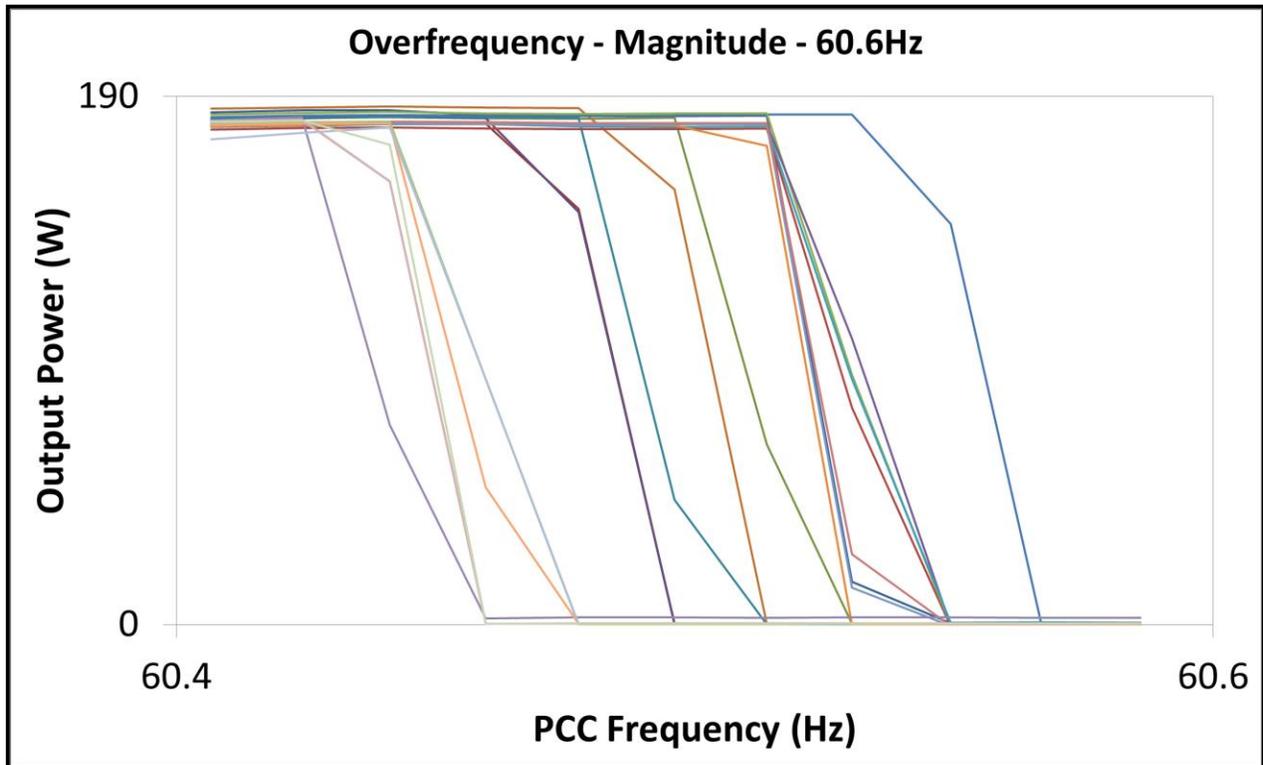


Figure 8. Overfrequency magnitude test results, 60.6 Hz.

2.2.2. Test for overfrequency – trip time (>60.5 Hz)

For the overfrequency trip time tests, a function was executed through the Grid Simulator to ramp the voltage up to 60.6 Hz and hold it there for 0.16 seconds to observe the trip time of each unit for the overfrequency level, repeated 4 times. The standard trip time limit is 10cycles/0.16s for frequencies >60.5 Hz [1]. Figure 9 shows the respective waveform plots of the individual string currents with trigger signals indicating the starts of each step in the frequency function for the overfrequency trip time test. Each string tripped well before the frequency reached 60.6 Hz.

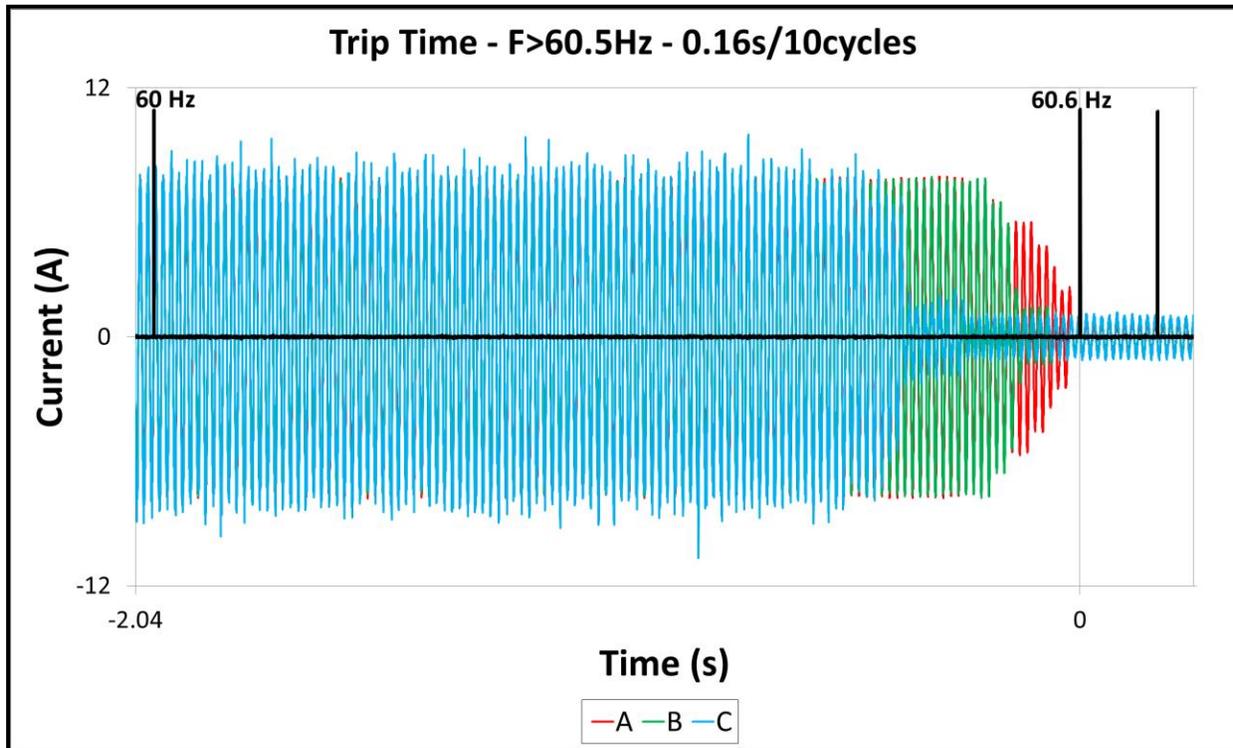


Figure 9. Overfrequency trip time test results, 60.6 Hz.

2.2.2. Test for underfrequency – magnitude (<59.3 Hz)

For the underfrequency magnitude test, a function was executed through the Grid Simulator to ramp the frequency down to 59.2 Hz as measured on the PCC voltage and observe the trip frequency magnitude of each unit, repeated 4 times. Figure 10 shows a plot of the individual microinverter real power outputs versus the decreasing PCC frequency. All units tripped above the 59.2 Hz threshold.

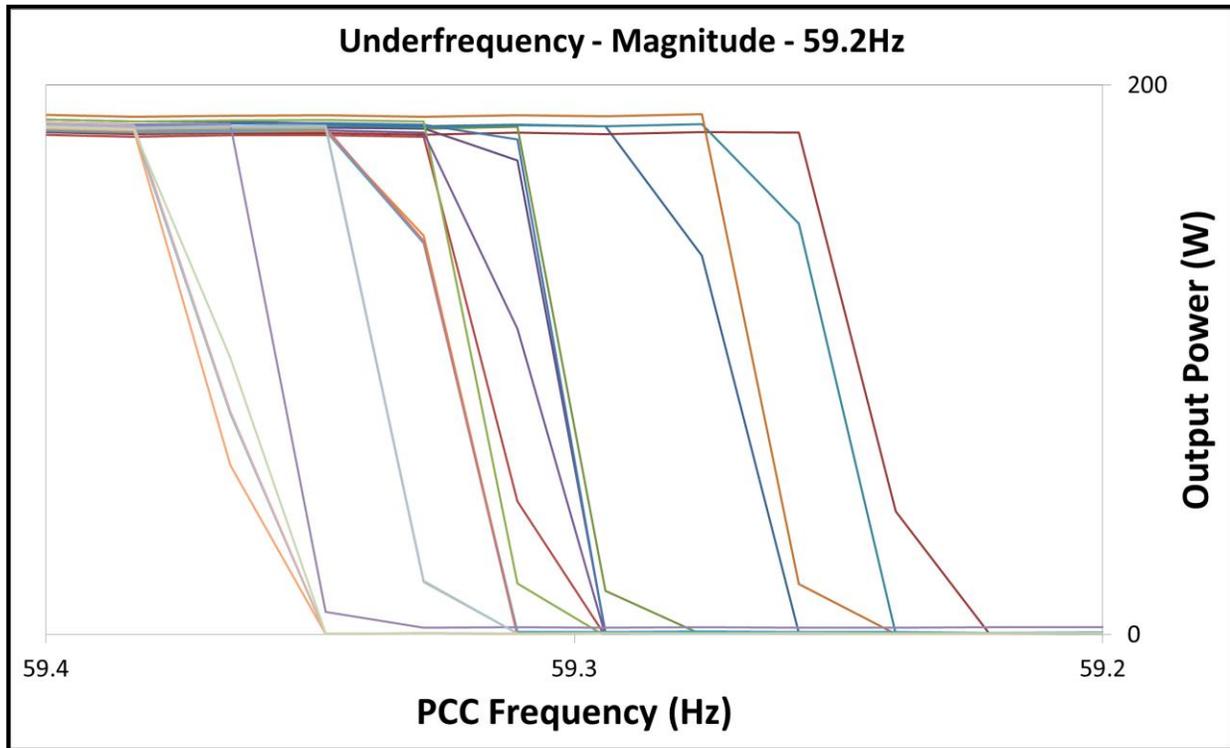


Figure 10. Underfrequency magnitude test results, 59.2 Hz.

2.2.2. Test for underfrequency – trip time (<59.3 Hz)

For the underfrequency trip time tests, a function was executed through the Grid Simulator to ramp the voltage down to 59.2 Hz and hold it there for 0.16 seconds to observe the trip time of each unit for the underfrequency level, repeated 4 times. The standard trip time limit is 10cycles/0.16s for frequencies <59.3 Hz [1]. Figure 11 shows the respective waveform plots of the individual string currents with trigger signals indicating the starts of each step in the frequency function for the underfrequency trip time test. Each string tripped well before the 0.16s/10cycle limit.

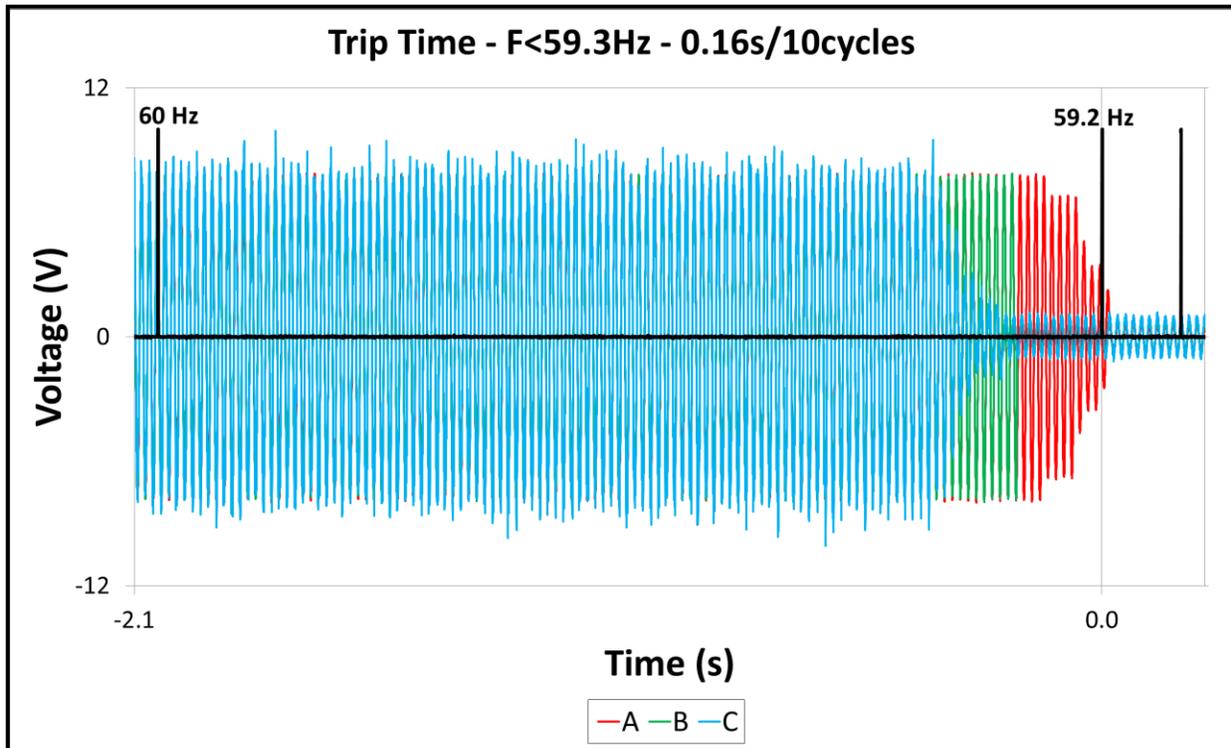


Figure 11. Underfrequency trip time test results, 59.2 Hz.

2.3. Unintentional islanding

The tests for unintentional islanding are specified in IEEE 1547.1, Section 5.7. The tests determined if the microinverter units cease to energize the grid within 2 seconds when an unintentional island condition is present. The tests are recommended at 33%, 66%, and 100% of rated power.

Since the testbed power output is at the mercy of outdoor conditions, the 100% and 66% test levels required timing both within the seasons and days to perform the tests near the desired test levels. The 33% power level tests were performed using a mesh shading material laid uniformly across the testbed modules [6]. The mesh allowed for capture of the 33% output level at more convenient times of day and during periods of lower rate of change of irradiance conditions, which occur closer to solar noon.

A tolerance of $\pm 5\%$ was implemented around each test level and all tests were repeated a minimum of 4 times. The trigger signal displayed in each plot coincides with the opening of the contactor between the testbed/load bank and the grid. There is an approximately 3 ms lag between the actual opening of the contactor and the acquisition of the trigger voltage through instrumentation, which is visible in cases where a string current appeared to trip prior to the opening of the contactor. The 3 ms lag adjustment would not have revealed any generation beyond the required trip limits.

Each islanding test was performed using the grid through the AC disconnect and the configurable RLC load for power output matching. A power harmonics analyzer was used to monitor the configuration of the load to consume the real power output of the system while creating the 60 Hz resonant frequency between the capacitive and reactive loads adjusted for a $Q=1$ [5]. Figure 12 shows the results of a 100% power output level islanding test, where the output was measured to be 103.3% or 4997.7/4836 W just before the time of disconnection from the grid. All units tripped in less than 0.05s after the loss of the grid. This is well below the 120cycles/2s requirement.

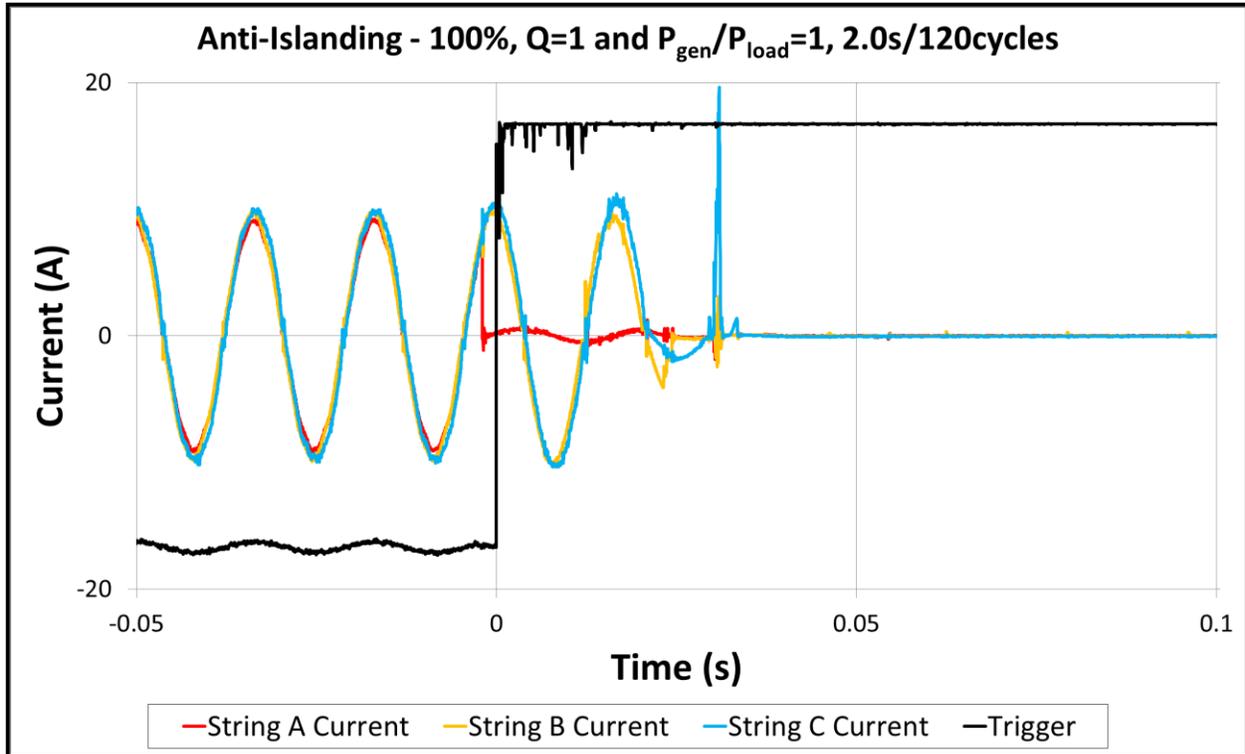


Figure 12. Unintentional islanding test, 103.3% of rated system power output.

Figure 13 shows the results of a 66% power output level islanding test, where the output was measured to be 65.6% or 3172.6/4836 W just before the time of disconnection from the grid. All units tripped in less than 0.1s after the loss of the grid. This is well below the 120cycles/2s requirement, although slightly more than was observed in the 100% level tests.

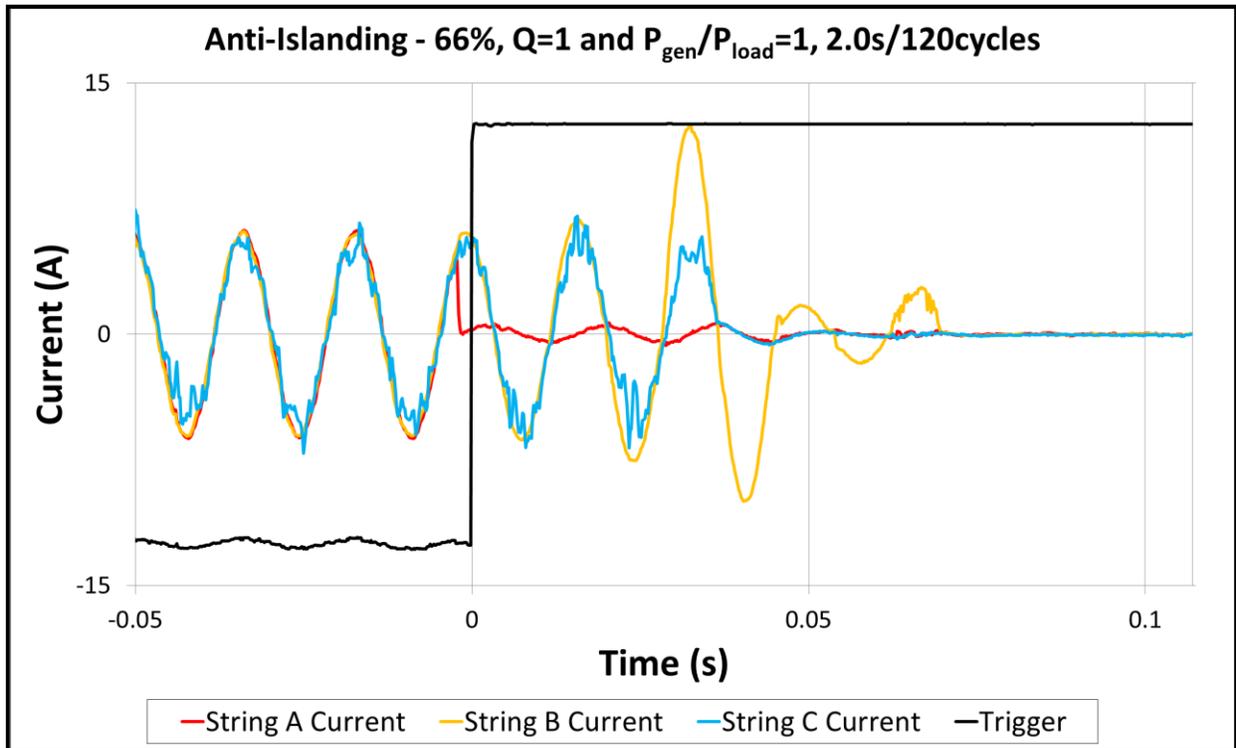


Figure 13. Unintentional islanding test, 65.6% of rated system power output.

Figure 14 shows the results of a 33% power output level islanding test, where the output was measured to be 32.2% or 1559.6/4836 W just before the time of disconnection from the grid. All units tripped in less than 0.15 s after the loss of the grid. This is well below the 120cycles/2s requirement, although slightly more than was observed in the 100% and 66% level tests. Lower power quality is also visible at this level, where it is common to see inverters employ lower frequency switching to increase energy harvest. This likely may have affected the island detection times as seen in the plot.

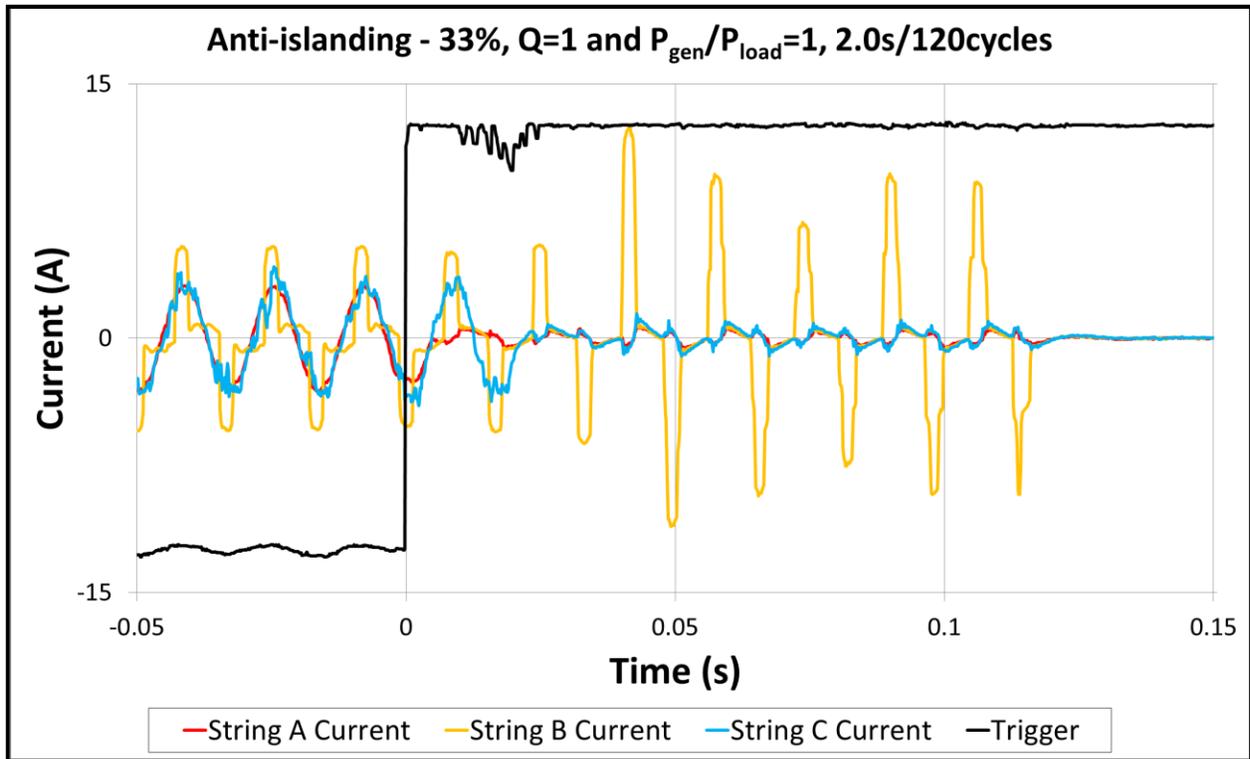


Figure 14. Unintentional islanding test, 32.2% of rated system power output.

2.4. Harmonics

The tests for harmonics are specified in IEEE 1547.1, Section 5.11. The tests determined if the testbed as a whole maintained harmonic current injections at levels below required thresholds for total demand distortion (TDD) and individual harmonic order percentages at 100% of rated current output.

Figure 15 shows the system current total harmonic distortion (THD) percentages as a function of output power. The levels from about 33% to 100% are well below the 5% limit defined in the standard. The standard does not define power quality limits for power outputs below 33%.

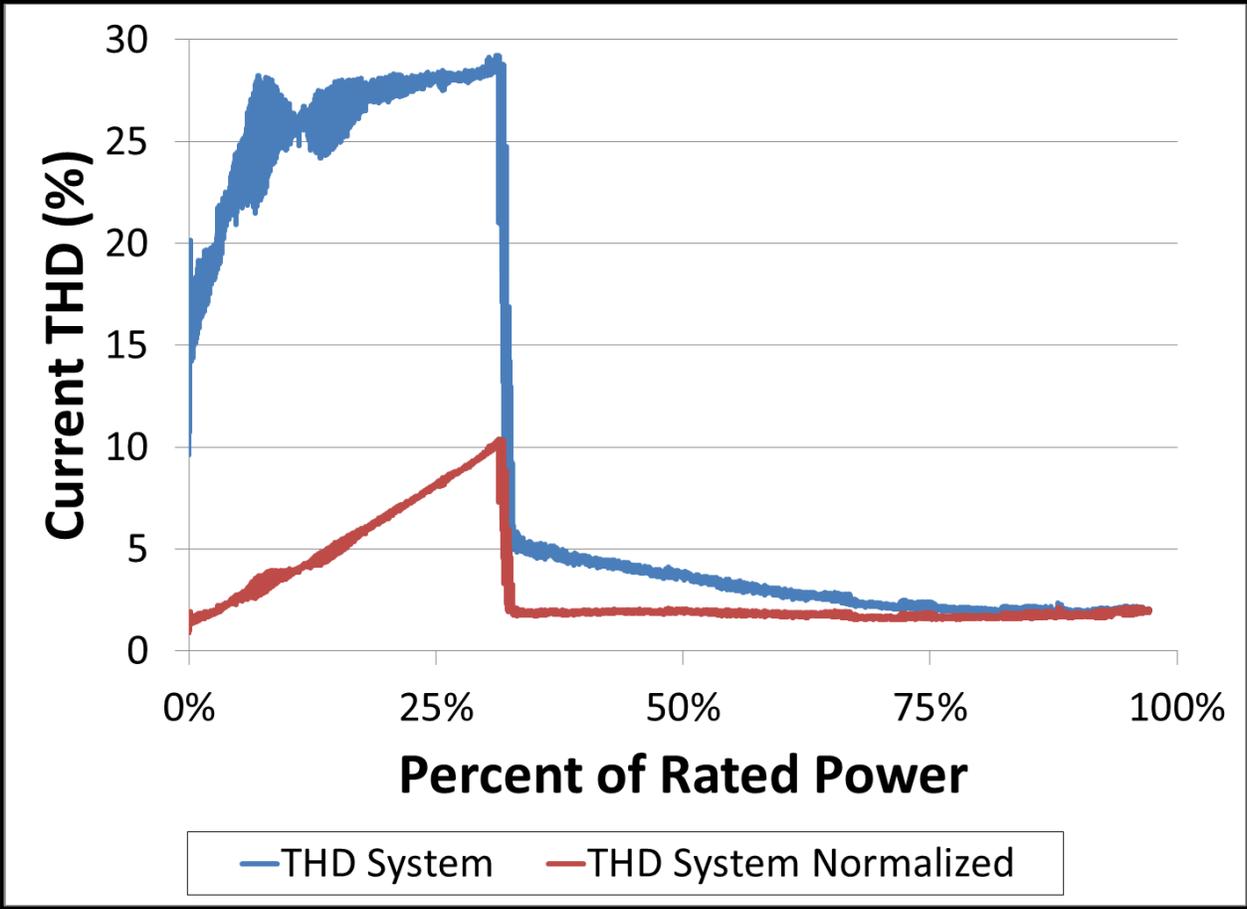


Figure 15. Total system current THD vs. output power, measured and normalized.

The standard defines the limits shown in Table 3 for each individual harmonic order [1]. Figure 16 shows the system current individual harmonic order percentages up to the 50th harmonic order while near 100% of rated current, colored by order groupings in Table 3. All levels were within limits.

Table 3. Maximum harmonic voltage distortion limits.

Individual harmonic order	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$
Percent (%)	4.0	2.0	1.5	0.6	0.3

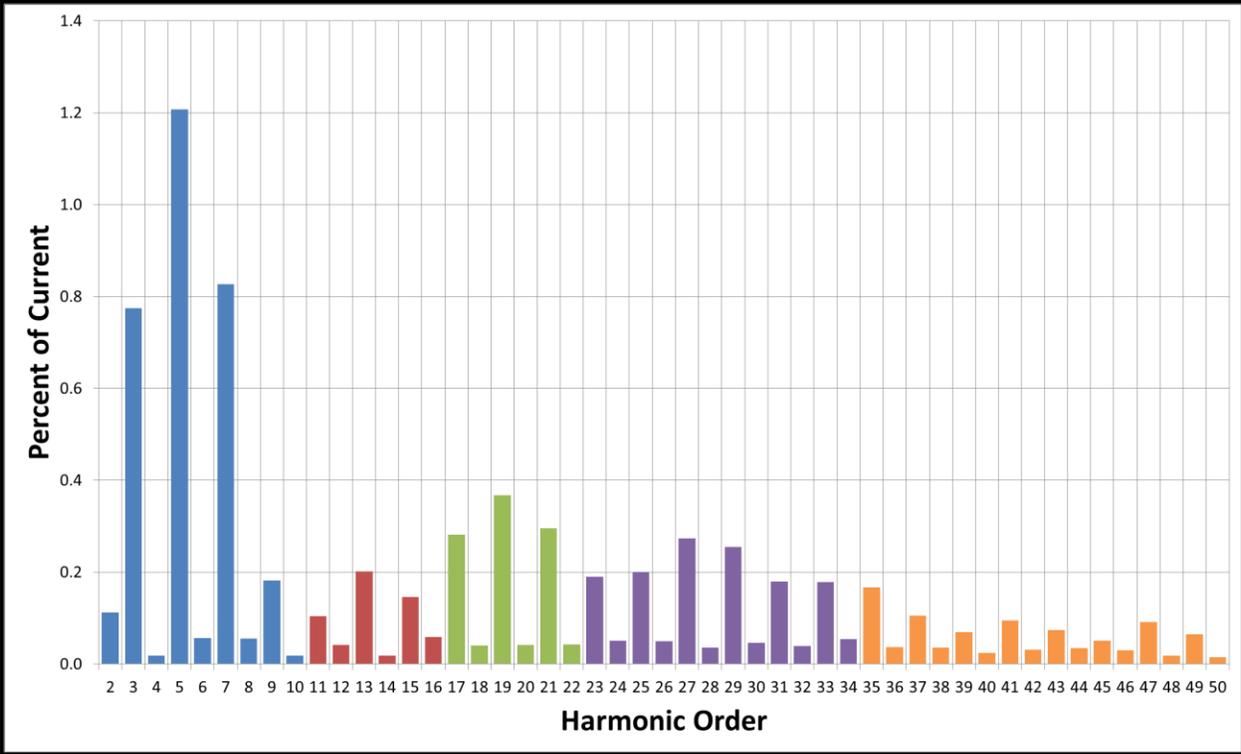


Figure 16. Total system current individual harmonic order percentages.

3. CONCLUSIONS

The microinverter isn't new to the solar industry, but the growth and implementation has gained significant momentum, fueled by the several favorable attributes inherent to the microinverter topology. These attributes include the mitigation of DC BOS requirements, eliminating the presence of high DC voltage, reducing exposure to DC voltage (favorable for new NEC 690.12 rapid shutdown requirements), and the reduction of the impact that module mismatch and shading has on the power generation of a PV system. While these attributes can have a significant impact on issues prevalent on residential PV installations, implementation can only be possible if microinverters can successfully interoperate with each other and the grid, and still meet grid standards.

The test results obtained in this study indicate that there are no issues caused by the interconnection of several microinverters, even when they are of different manufacture. The voltage magnitude tests revealed generation beyond the standard thresholds as a result of microinverter measurement accuracy. While this is considered acceptable for certification testing [4], situations requiring stricter adherence to the thresholds may require better measurement accuracy and/or device trip setting adjustment. The potential risks of generation beyond these points to the levels observed were also beyond the scope of the project.

Additional tests beyond those studied in this project will become essential to an interoperability assessment of microinverters as technology advances toward more advanced inverter control, such as those being evaluated for California Rule 21 [7]. These may include at least all test aspects highlighted in this report with advanced functionalities enabled, such as voltage and frequency ride through and volt/VAr control. Control parameters will need to be established, as well as test protocols to thoroughly assess interoperability. SNL is taking initiatives to develop and implement such protocols, such as the *Test Protocols for Advanced Inverter Interoperability Functions – Main Document* [8], on both string inverters and microinverters.

4. REFERENCES

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