MICROSCALE C-SI (C)PV CELLS FOR LOW-COST POWER

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ABSTRACT

We are exploring fabrication and assembly concepts developed for Microsystems/MEMS technology to reduce the cost of solar PV power. These methods have the potential to reduce many system level costs of current PV systems including, among others, silicon material costs, module assembly costs, and installation costs. We have demonstrated a direct c-Si material reduction of approximately 20X (including wire-saw kerf loss and polishing loss). The cells have achieved efficiencies of almost 9% and J_{sc} of 30 mA/cm^2. We are currently using integrated-circuit (IC) fabrication tools that will lead to higher efficiencies and improved yield. These advantages and the material reduction are expected to reduce the current module manufacturing costs.

1. INTRODUCTION

Standard single-crystal or multi-crystalline solar cells consume approximately 380 to 400 microns of material of the ingot (combining wafer thickness, polishing loss, and kerf loss). Thin silicon photovoltaics have advantages over their thick counterparts such as increased spectral response, open circuit voltage (V_{oc}), and fill factor (FF); mainly due to a decreased bulk recombination [1]. Among the approaches found in the literature to create thin crystalline silicon films are: film growth on native substrates [2-3]; film growth on foreign substrates (like glass); and techniques that create a thin film separately from the wafer (which will be the starting material) either by layer transfer or lift-off [4,5].

Thin starting material (<50 μm thick) may be used to reduce the amount of silicon that is required for PV cell fabrication [6]. However, thin semiconductor layers resulting from these techniques require unique fabrication techniques to create the final PV cells. Large areas (>1mm across) of thin silicon are fragile and thus hard to handle and process under normal solar cell procedures.

Two newly developed methods have been demonstrated in which the p-n junction is fabricated before obtaining a thin layer. The first approach is the one used to produce Sliver® cells [7,8]. In this method, the junction is created in 0.5-2 mm thick wafers; the wafer is then processed to form narrow, parallel trenches through the thickness of the wafer, perpendicular to the wafer surface. Once the processing is finished; the Sliver® cells are released from the frame, interconnected, and encapsulated into a module. The second approach creates thin PV cells transferred to a substrate with an elastomeric stamp [9]. The cells are of a long rectangular shape and are processed and defined through lithographic steps. This is followed by a partial under-etch that leaves the cell "anchored" to the wafer. The electrical interconnection is done and finally a stamp adheres to the cells and breaks them free from the wafer. The stamp provides a receiving substrate for the cells. Both approaches lead to cells with thicknesses from 20μm to 50 μm.

By using processes that have been adapted from microelectromechanical systems (MEMS) technologies, we have created 14-20 μm thick layers of c-Si with p-n junctions that function as PV cells (see Fig. 1). Our approach performs as many steps as possible on full thickness wafers, allowing direct use of currently available manufacturing tools. In this scheme doping, diffusion, and metallization steps are performed before separating the devices from the c-Si wafer substrate.

These cells are designed to be very small, on the order of several hundred microns across. This small form factor allows the use of self-assembly methods that use energy minimization concepts for the placement of small die onto a substrate. The benefits of this approach include significant reduction of c-Si usage, the use of inexpensive "roll-to-roll" module manufacturing available to thin-film PV manufacturing, and high-efficiency and high-reliability possible with c-Si PV cells. We will also be able to use concentration to further reduce costs (either low-concentration with non-tracking or high-concentration with tracking).

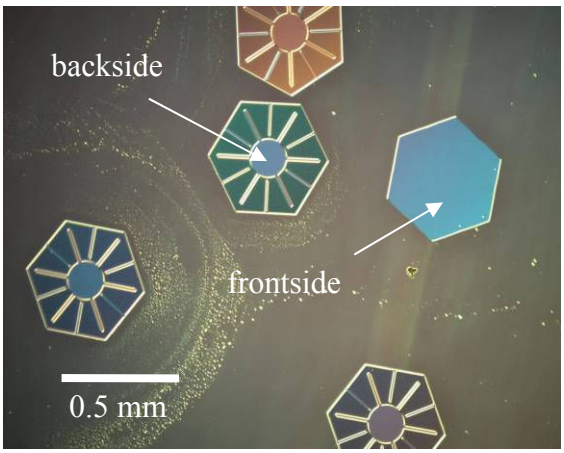

Fig. 1. Optical image of 500 micron wide, 20 micron thick cells.

2. CELL FABRICATION

The process to create arbitrarily thin crystalline silicon PV cells uses standard integrated circuit fabrication techniques combined with MEMS release techniques. The cells are created using standard processing steps followed by a deep etch to define the dimensions of the cells. While we are using lithography, implantation, and reactive ion etching (RIE), laser machining and spin on dopants could

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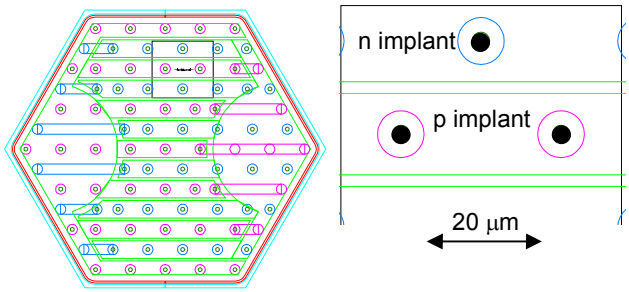

Fig. 2. Design of a 250 μm cell and point contact zoom of a KOH released cell. The black dots are the point

also be used to create the trenches and diffusions respectively. The release is achieved by an oxide etch or crystal plane selective etch as described below. In both approaches, a significant benefit in energy and material costs can be realized by using gaseous feedstock and epitaxy with wafer reuse, thus eliminating polysilicon and ingot growth and wire-saw steps which are necessary in standard wafer consuming processes.

The first method uses silicon-on-insulator (SOI) wafers (bought from SOITEC) that have a buried silicon dioxide sacrificial layer. The wafer has a device layer that is 20 μm thick and a buried oxide thickness of 1 μm. To create the junction, we have used both solid source diffusion and ion implantation of dopants through lithographically masked 0.8 μm thick LPCVD low stress nitride layer. Both aluminum (with and without titanium silicide) and CVD tungsten have been used for the metal contacts. The wafer then is placed in a HF based chemistry bath to selectively etch the buried oxide. The PV cells are released from the substrate and collected in solution for assembly.

The second method began with a p type (111) oriented silicon wafer. Conventional photolithography was used to pattern the windows for dopant implantation. The implantations of boron (energy = 45 keV) and phosphorus (energy = 20 keV) were done with a dose of $1X10^{15}$ cm^{-2}, tilt of 7°, and range of 0.15 μm. A drive-in step was done for 30 minutes at 900°C in N_2 atmosphere. Fig. 2 illustrates the sizes and separation of diffusions and contacts inspired from the design proposed by Swanson et. al [10]. Once the junction was formed, a deep trench was etched to the desired cell thickness using deep reactive ion etching (DRIE), followed by a conformal deposition of low stress silicon nitride that protects the walls. The nitride was then photopatterned and reactive ion etched (RIE) to create windows for point contacts to the implanted areas. The metallization step was accomplished with a 200 nm thick CVD tungsten film deposited on top of 50 nm of TiN to improve adhesion. The metal was patterned by lithography and RIE. Next, a second DRIE etch created the access point for the KOH chemistry. Finally, the wafer is etched in a KOH chemistry to release the cells by laterally undercutting in the preferred silicon crystal etch direction. All other areas are protected from the release chemistry by low-stress silicon nitride. Fig. 3 illustrates both the first and the second

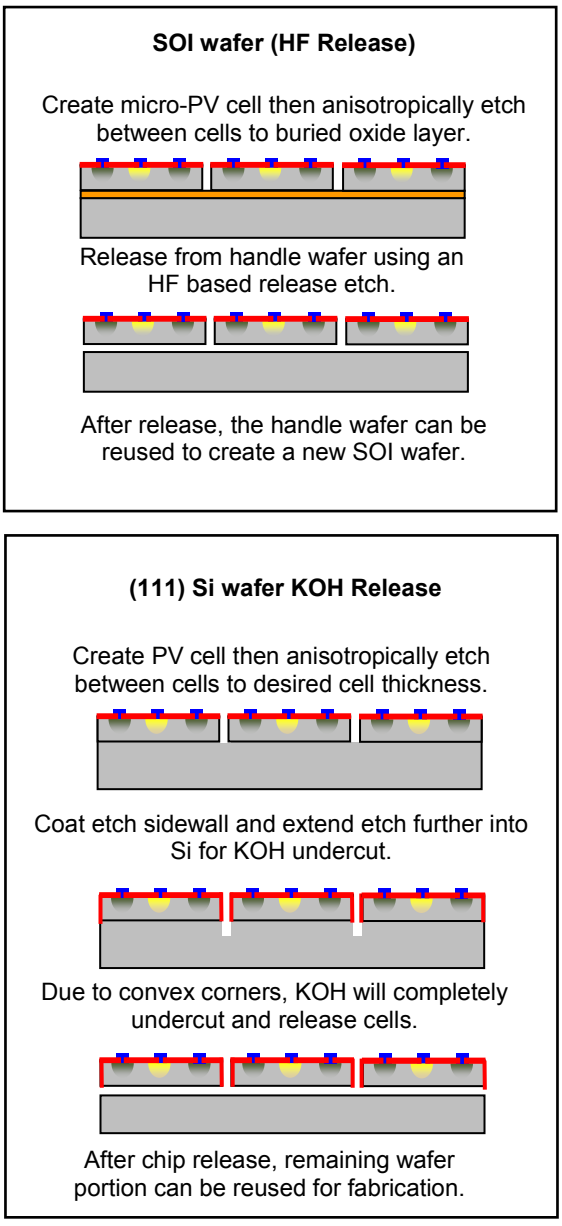

Fig. 3. SOI and (111) oriented wafer methods of creating and releasing thin PV cells.

method. Electrical characteristics of this device with subsequent passivation are shown in Fig. 4.

Release Chemistry

For the SOI cells, the wafer part was etched in a 49% HF solution containing Tergitol (a non-ionic surfactant) which was used to aid in wetting the Si surface. The device side faces down so that the parts would fall off of the substrate once the buried oxide was removed. The etch time was determined by how long it took for most of the various size PV cells to fall off of the substrate. The etch time varied

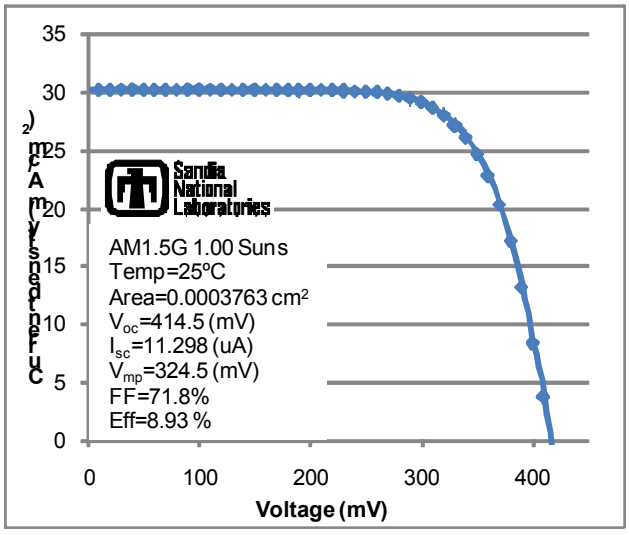

Fig. 4. IV curve of an individual cell tested under standard conditions.

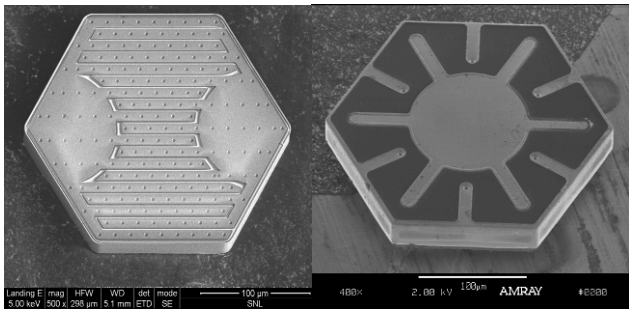

Fig. 5. SEMS of released cells. The left design is a cell released using a KOH anisotropic etch and the right design is a cell released using the SOI approach.

from 30 to 90 minutes. The release solution was filtered to capture the lifted PV cells. Deionized water was flushed through the filter until the rinse water was pH neutral. The lifted PV cells were then rinsed out of the filter into a glass bottle with isopropyl alcohol.

For the KOH wafer release, the wafer substrate was etched in 6M KOH at 85°C for 3.5 hours (with the parts facing down) until the PV cells fell off of the substrate. The KOH was then filtered to capture the lifted PV cells. Deionized water was flushed through the filter until the rinse water was pH neutral. The lifted PV cells were then rinsed out of the filter into a glass bottle with isopropyl alcohol.

We have successfully created 14-20 µm thick silicon cells using both techniques. The yield for the release is almost 100% for both cases. These cells have backside contacts, illustrated in Fig. 5, to eliminate shading of the cells. These cells have been tested and have shown photovoltaic functionality.

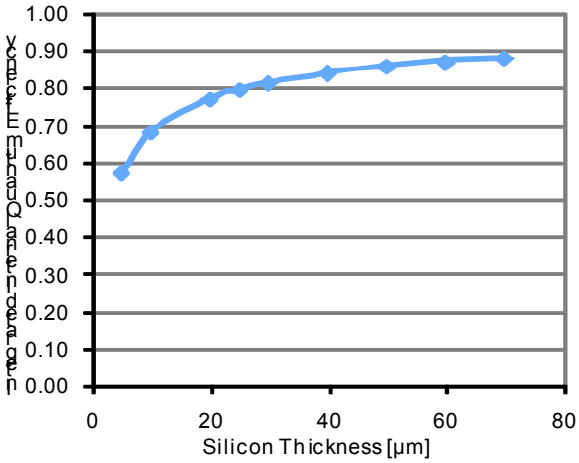

Fig. 6. Simulated integrated internal quantum efficiency of cells versus silicon thickness.

We anticipate that due to the use of higher quality fabrication tools (i.e. IC tools), the yield of the cells and the efficiency of the cells will be high, which is a trend that has been observed in earlier device development efforts.

To achieve high efficiency with these cells, a number of things need to be addressed. First, the cells need a high-quality passivation layer. Surface passivation becomes more important as the wafer thickness is reduced due to the increased surface to volume ratio [11]. Ultra-thin (<40 µm) cell performance is dominated by surface recombination. This is a significant challenge since the release surface is bare silicon. We are exploring using a buried silicon nitride layer to passivate that surface for the silicon on insulator (SOI) released cells. However, that method is not an option for the (111) silicon cells.

Post treatment of the front surface with proven passivation methods is possible. Passivation films can include silicon oxide, silicon nitride, and alumina. We are experimenting with depositing silicon nitride using plasma enhanced chemical vapor deposition (PECVD) and alumina using atomic layer deposition (ALD) on released cells for passivating layers. Thermally grown SiO_2 is a high-quality passivation layer but it requires a high temperature treatment which could damage the junction and the metallization. PECVD has demonstrated good passivating films but careful tuning of all the variables for the film growth (pressure, temperature, flow of gases, frequency, and power) and the required post-deposition anneal (time and temperature) for the cell is required [12]. ALD alumina has not been thoroughly developed but some researchers have achieved passivation comparable to thermal oxides [13].

We are also working on developing a good anti-reflective (AR) coating for the released surface. This may be addressable through the passivation layer. Silicon nitride has a nearly ideal refractive index and PECVD deposition allows additional tuning of the index from 1.8 to 2.3 by varying the concentration of the gases inside the growth

chamber. ALD alumina has a relatively constant index of about 1.6 when deposited at 200°C [14], resulting in a thicker film requirement for an AR coating.

Due to the very thin nature of these cells, light trapping is an important consideration. However, cell simulations show that the integrated internal quantum efficiency of the cells should be near 80% with a single pass through a 20 μm thick cell (see Fig. 6). In addition, we are considering methods to increase the optical absorption within the cell accomplished by increasing the optical path length of the light. Several efforts are reported in the literature: random textures, geometrical structures, and external optical elements [15]. The texture scatters the light entering the cells and causes the light to bounce several times inside the device before exiting. We intend to explore a variety of geometries, and technologies to create these geometries, to increase the optical path length inside the cells.

Finally, the design of the cell junction is crucial to achieve high efficiencies. Critical parameters include the size of the doped regions; the doping profile of the diffusions; the contact design, distribution, and size; the thickness of the cell; and others.

We have created solar cells with good IV characteristics with our initial efforts at passivation. Fig. 4 shows the IV behavior from a 250 μm diameter, 14 μm thick cell released using a KOH anisotropic etch. The passivation/antireflection process used PECVD to deposit a thin layer of silicon oxide followed by silicon nitride. The sample was then annealed at 430°C for 2 hours.

3. MODULE ASSEMBLY

We are designing the cells to allow massively parallel assembly techniques to allow very low cost module manufacturing [16,17]. Self-assembly is a technique that encompasses a wide variety of approaches to make a part of interest move to and stay in a desired receiving spot. All approaches take advantage of energy minimization in the system. Some of the principles used to generate self-assembly are molecular interactions [18], electrostatic forces [19], capillary and surface tension interactions [20], magnetic forces [21], and even DNA molecules [22]. Through the use of self-assembly, many cells can be assembled at once on the module. This will significantly reduce module assembly costs.

A wide variety of substrates can be used for device assembly due to the fact that the high temperature steps required to create the PV cell are fully complete before the cell is assembled on the substrate. Not only does this allow low-cost substrates to be used for the modules, it can potentially enable many building-integrated PV (BIPV) concepts.

4. COST ANALYSIS

Even though crystalline silicon is a strong candidate to produce reliable and high efficiency solar panels with long life, the price of this technology is still not competitive with current grid power (2-4 times more expensive) [23]. From the cost breakdown of the silicon PV systems (see Fig. 7) [24], one can see that half of the system cost is due to the module itself and almost a quarter of the cost is just the wafer. In order to reduce costs, a reduction of the amount of material used for solar cells is crucial. This can be accomplished by using high-efficiency, ultra-thin silicon structures and/or concentration. However, if the vision of this work is successful, not only will material costs be reduced; there will also be significant module and system cost reductions.

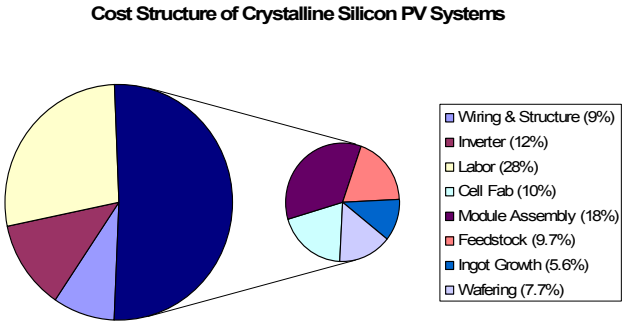

Fig. 7. Breakdown of costs associated with crystalline silicon module PV systems.

Utilizing cost assumptions for silicon integrated circuit processing technologies, we have generated several scenarios based on cell efficiency, assembly cost, and concentration levels. The graph in Fig. 8 show the two cases for a 1 m^2 module assembly cost of $100 and $50 (roughly equivalent to the module assembly costs for c-Si and thin-film modules, respectively). Two cells with different conversion efficiencies are shown. In all cases, once a modest (~10-20x) level of concentration is reached; costs associated with silicon material and processing become relatively small. With a continuous, roll-to-roll assembly process, the final generated electricity cost for this technology is expected to move below the $1/Wp level. Further reductions in the cell fabrication costs are also possible by optimization of the tool and material costs for the IC cell processing steps.

5. CONCLUSIONS

The important benefits of these cells are the reduction in silicon usage and the new fabrication and deployment options enabled by this approach. Most of the solar spectrum is absorbed in the first 10-20 μm of silicon. Figure 5 shows the variation of integrated internal quantum efficiency of the cells versus silicon thickness obtained in device simulations. Further, the kerf loss of this method is at most a few microns of silicon per cell layer. This gives greater than a factor of ten savings in the single largest cost of solar modules and allows the creation of

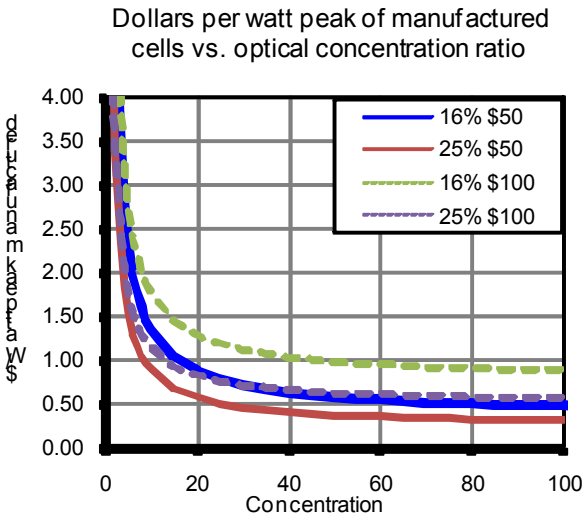

Fig. 8. Cost projections for $100/m^2 and $50/m^2 panel assembly cost. These assume 8 inch wafer production, 95% cell yield, 15% incoming light reduction due to diffuse light, 6% optical loss (lens) and standard silicon processing tools.

modules with << 1g Si/W_p. In addition, there are unique module and system level benefits that result from utilizing the small dimensioned solar cells which further reduce the

module and system level benefits that result from utilizing the small dimensioned solar cells which further reduce the cost of the PV modules and systems. So far, cells tested under 1 sun have achieved almost 9% conversion efficiency with a V_{oc} of 414 mV and, a J_{sc} of 30 mA/cm^2, and a FF of 72%.

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