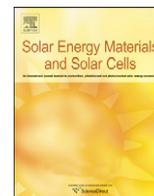




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Microsystems enabled photovoltaics: 14.9% efficient 14 μm thick crystalline silicon solar cell

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ABSTRACT

Crystalline silicon solar cells 10–15 times thinner than traditional commercial c-Si cells with 14.9% efficiency are presented with modeling, fabrication, and testing details. These cells are 14 μm thick, 250 μm wide, and have achieved 14.9% solar conversion efficiency under AM 1.5 spectrum. First, modeling results illustrate the importance of high-quality passivation to achieve high efficiency in thin silicon, back contacted solar cells. Then, the methodology used to fabricate these ultra thin devices by means of established microsystems processing technologies is presented. Finally, the optimization procedure to achieve high efficiency as well as the results of the experiments carried out with alumina and nitride layers as passivation coatings are discussed.

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1. Introduction

Reducing the amount of photovoltaic material used in solar cell production is a common goal for the solar cell industry, due to its significant contribution to the overall cost of a photovoltaic (PV) system. Depositing thin films on inexpensive materials, thinning the wafers, or using small cells in combination with concentration optics are approaches taken to minimize the use of the active semiconductor material.

Systems based on silicon wafers are currently the dominant technology of the PV market [1]. Thus, in this paper, we present a wafer compatible fabrication solution that saves up to 30 times the amount of silicon used (including Kerf loss) as compared with current crystalline silicon (c-Si) photovoltaic modules. This paper presents the design, simulation, fabrication, optimization, and testing of sub-millimeter and ultrathin solar cells.

Previous research efforts in the industry and academia have shown interest for creating thin wafers. As a proof of concept, a

47 μm thinned wafer using a passivated emitter with rear locally diffused design (PERL) was able to obtain an efficiency of 21.5%. [2] Since the wafer was thinned, this technique did not save material. Another technique, called direct transfer [3] produced 13.2% efficient solar cell with 40 μm thick wafers. This technique saves material through hydrogen assisted cleaving, releasing only the first thin layer. Other groups [4] proposed a thermo-mechanical process able to release silicon foils with a thickness between 30 and 50 μm in a relatively large area (25 cm^2). Efficiencies around 10% were reported. The disadvantages of such thin wafers are the handling challenges introduced when processing them with standard fabrication tools.

Another approach is using small silicon cells in conjunction with concentration optics to create low profile concentration modules with highly efficient solar cells from standard thickness wafers. In one technique [5], the die are cut with a saw into $2.3 \times 2.3 \text{ mm}^2$. In order to reduce recombination at the sawed edges, they are heavily doped to create an electric field that repels carriers. This technique produced 18.4% efficient cells, with a regular thickness. Currently, the record for silicon cells under concentration is at 27.6% using a small 1 cm^2 back contacted cell under 92 suns [6]. Small silicon cells of standard thickness are currently used by the industry to create low concentration, low profile modules [7].

Other efforts combine using thin substrates and small cells [8]. These efforts report the production of small lateral dimension rectangular silicon cells with efficiencies between 4% and 10%,

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thicknesses from 20 to 50 μm , widths around 1 mm, and lengths of several centimeters. However, these cells lack high efficiencies and standard manufacturing procedures. Other researchers have used micromachining techniques to create thin silicon cells that are about 50 μm thick, 0.5–1 mm wide, and several centimeters long with efficiencies up to 20.1% [9,10].

Microsystem enabled photovoltaics (MEPV) is a new approach [11] that uses tools and concepts used in the integrated circuit (IC) and microsystems arena to create and release inexpensive, sub-millimeter, ultrathin, back contacted, and highly efficient solar cells. Using standard tools and processes employed in silicon IC fabrication potentially leads to several advantages such as a mature and scalable material base, higher yields, and processing know-how. Furthermore, the use of processes to create small and thin cells potentially leads to improved carrier collection [12], no shadowing and simple connections due to back-side contacting design, high open circuit voltage (V_{oc}), significant reduction in material use, handling wafer reuse, and increased utilization of wafer edges. Recent MEPV research by our group has shown a reduction in the amount of silicon material used by a factor of 30 (including Kerf loss) on 250 μm diameter cells while attaining efficiencies as high as 9% [13]. Further advantages at the module and system levels have also been reported with the help of micro-concentrators and self assembly [14].

2. Design of the cell

Our cell designs are similar to the point-contact, back contacted crystalline silicon solar cells proposed by Sinton et al. [15]. Key differences exist in the scale and geometry of the cells presented here with sub-millimeter lateral dimensions and thicknesses on the order of tens of microns. Back contacted solar cells are desirable because they have no metal shading losses and allow coplanar interconnection. Another advantage of these cells is that they can have the back junction optimized for electrical performance and the front surface optimized for optical performance independently of each other [16].

The cell design consists of a set of alternating p and n implanted, doped regions contacted through an interdigitated metal structure. Fig. 1 shows a sketch of the thin, back contacted, silicon solar cell with details of the back (contacting) side as well as cross sectional views. Cross section 1–1' shows alternating p and n doped regions. Cross section 2–2' shows the elongated n doped region while cross section 3–3' shows the elongated p doped region. More details on the fabrication are shown later.

The elongated n regions are buried below a nitride layer under the p metal layer and the elongated p regions are buried below a nitride layer under the n metal. Both elongated implanted sections are only contacted at the edge of the finger to avoid shorts on the opposite polarity metallization. The purpose of these regions is to improve carrier collection under the metal contacts. Note that the design of the cell includes an integrated nitride passivation layer on all sides except the front of the cell. The top and side nitride protects the cell during release etch.

All the patterns are defined by conventional photolithography and the masks used were designed using AutoCAD design software. A total of 5 photolithographic masks were used to create our solar cells. The first defines small circular p implantation areas, the second defines the n implantation areas, the third mask serves a dual purpose defining the lateral size of the cell as well as a deep trench that allows the release, the fourth defines the point contacts from the metal to the implanted areas through the passivation layer, and the fifth defines the interdigitated metal pattern.

The influence of surface recombination on ultra-thin cells was explored through modeling. The tools used to simulate the

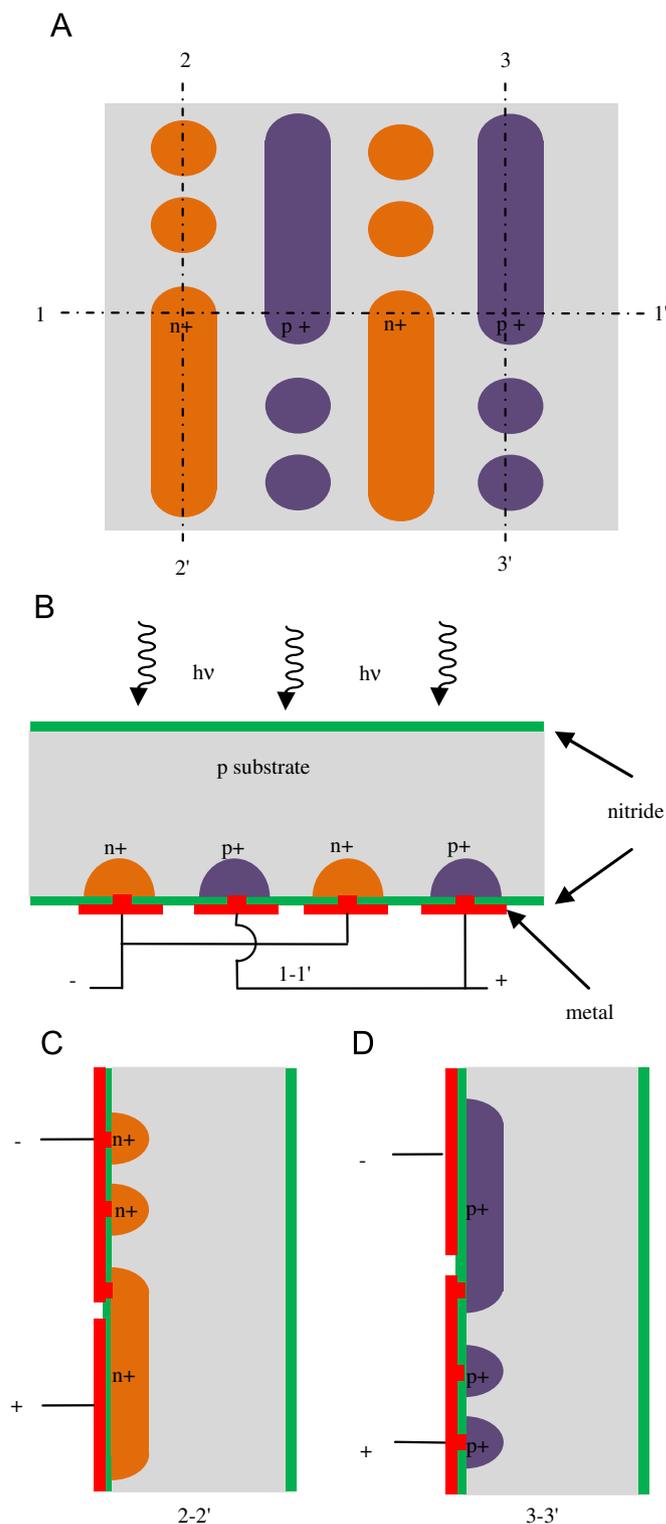


Fig. 1. (A) Backside of the solar cell showing the n and p doped regions (the metal and nitride layers are not displayed in this view). (B) Cross section 1–1' of the cell showing the alternating p and n doped regions. (C) Cross section 2–2' showing the long n doped region. (D) Cross section 3–3' showing the long p doped region.

fabrication process and electronic characteristics of the device are Tsuprem4 and Medici, respectively (available from Synopsys). Process steps that can be simulated include implantation, diffusion, oxidation, etching, deposition, lithography, and epitaxy. The output of Tsuprem4 is a two dimensional cross section of the device. The output also contains information about the strains in layers,

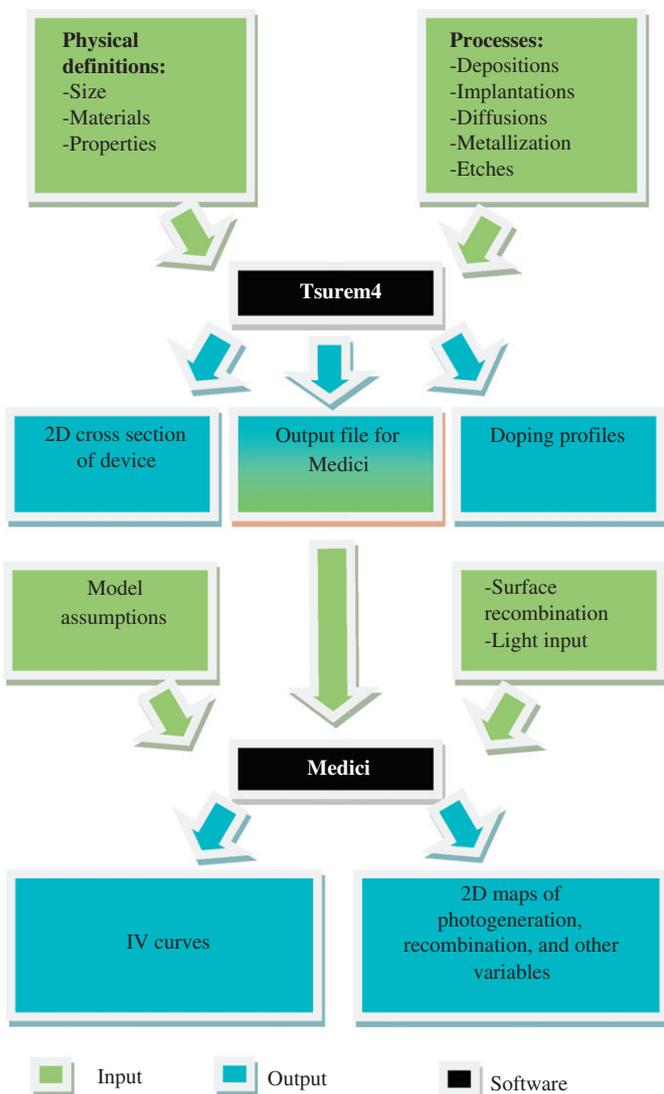


Fig. 2. Block diagram of the simulation steps in TSUPREM4 and MEDICI.

with the default software values of the Auger coefficients $2.8 \times 10^{-31} \text{ cm}^6/\text{s}$ for electrons and $9.9 \times 10^{-32} \text{ cm}^6/\text{s}$ for holes. The continuity equation for holes and electrons together with the Poisson equation are solved simultaneously by the software to obtain the current and voltage characteristics.

Surface passivation has a very strong effect on cell performance in micrometer sized cells due to the proximity of surfaces to active regions of the device. Atoms at surfaces have incomplete bonds (dangling bonds) that act as carrier traps and degrade device performance. Surface recombination velocity (SRV) expresses the quality of the surface passivation (slower velocities indicate better passivation). Furthermore, given the back contact nature of the cells, carriers generated near the surface have to diffuse (without the help of fields) through the thickness of the semiconductor. Here thinner cells have an advantage over thicker cells. Fig. 3 shows the cell model used in the simulations. It is a representative cross section that is repeated 6 times in a $250 \mu\text{m}$ wide solar cell in a 2D model. The top and bottom interfaces were modeled to have variable surface recombination and the sides were considered to have constant zero surface recombination since the repetition of the block along the horizontal axis is done several times across a real cell and the edges will be negligible in the simulation. The nitride is modeled as an optical layer with refractive index of 2.0 and a thickness of 70 nm in order to create an anti-reflection coating. The back metal is simulated as a reflecting substrate. In the simulations, we changed the surface recombination velocities from 0 to 10^5 cm/s while keeping the dimensions constant at $42 \mu\text{m}$ wide and $14 \mu\text{m}$ thick and characterized the variation in current–voltage characteristics. Efficiency numbers were calculated from these IV curves.

Fig. 4 shows the simulated JV curves by Medici. These curves demonstrate the effect of surface recombination velocity on the performance of the cell. It can be seen that SRV plays a crucial role in the performance (measured as efficiency). Moreover, since most of the carriers are generated near the front surface, passivation on this surface plays a vital role in preventing recombination. In the graph, the current and open circuit voltage are increased drastically as the SRV is reduced from 10^5 to 100 cm/s . An ideal case where the SRV is 0 cm/s was also plotted as a comparison.

The metal, present on 87% of the back of the cell, was set up in the simulations to act as a perfect reflector. In a planar device with a metal back reflector (like the one simulated), the light will

boundaries of different materials, and impurity distributions [17]. Medici is a device simulator capable of modeling the transient and steady state behavior of electrical, thermal, and optical characteristics of semiconductor devices created in Tsuprem4 [18]. Fig. 2 is a diagram explaining the implementation of these two tools in order to characterize the simulated device.

In the simulations, we assume a two dimensional block, back contacted, silicon solar cell section with implanted dopants and point contacts, which is representative of the whole solar cell. The assumed material was a (1 1 1) oriented silicon p-type wafer with background doping of $7 \times 10^{14} \text{ cm}^{-3}$ and a lifetime of $50 \mu\text{s}$. To simulate the p–n junctions, the same conditions as those used in the fabrication of the device were used. To obtain IV curves of the cell under illumination, we used a dataset representing the standard AM 1.5 solar spectrum truncated to wavelengths between 0.3 and $2.4 \mu\text{m}$ and divided into 100 points. The models used in the simulation assume a concentration dependent mobility at 300 K using software default tables at low fields for electrons and holes [19], a Shockley–Read–Hall recombination model with concentration dependent lifetimes, bandgap narrowing using a heavy doping model (Slotboom's bandgap narrowing) with values of concentration parameter = $1.3 \times 10^{17} \text{ cm}^{-3}$, voltage parameter = 5.21 mV , and constant parameter = 0.5 eV . Auger recombination is modeled

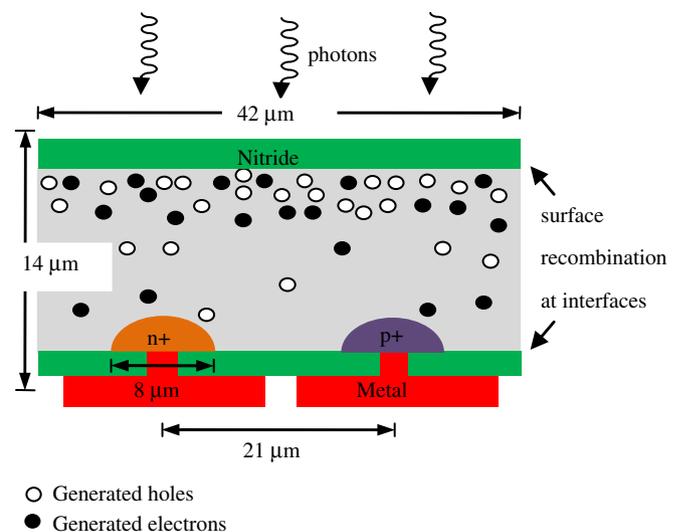


Fig. 3. Representative 2D cross section of the cell used in the simulations. Recombination and generation sites are shown. This block is repeated 6 times in a $250 \mu\text{m}$ wide solar cell. The front surface should possess the highest quality passivation possible since it is where most carriers are generated.

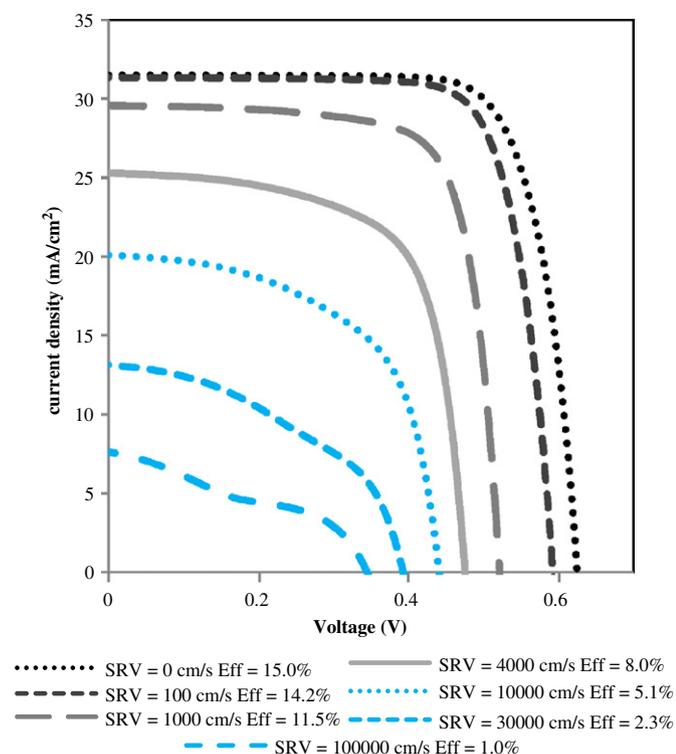


Fig. 4. Simulated JV curves of a 14 μm silicon cell with different surface recombination velocities (indicative of surface passivation quality).

do a double pass through the device – once on the way in and once after reflection from the back surface – allowing the cell to appear twice as thick. It should be noted that optimum light management structures have separately predicted to enable an efficiency of up to 20% for a 1 μm well-passivated solar cell [20]. With an engineered textured cell, the path length of the light (and thus absorption) is increased by multiple internal reflections. Techniques such as anisotropic etch using KOH on (1 0 0) oriented wafers or acid based chemical etches for other crystallographic orientations such as (1 1 1) are common techniques used by the solar cell industry to create textures on the cell substrate [21].

3. Fabrication, optimization, and characterization

3.1. Fabrication of the solar cell

The process begins by implanting alternating p and n type dopants into regions approximately 8 μm in diameter on a 6 inch, 700 μm thick, 3–20 Ω , CZ semiconductor grade, p type, (1 1 1) oriented wafer to create the junctions. Implantations of boron (energy=45 keV) and phosphorus (energy=120 keV) were done with a dosage of $1 \times 10^{15} \text{ cm}^{-2}$, tilt of 7°, and range of 0.15 μm for both dopants. A photolithography patterned 2.2 μm thick photoresist was used to selectively mask the implantations. A drive-in step was performed for 30 min at 900 °C in a N₂ atmosphere. The dimensions and separation of these implants can be seen in Fig. 3. After the junction is completed, five etches follow. Fig. 5 provides a process flow diagram. The first etch is a trench that defines the sides and depth of the cell; the second etch opens windows in a previously deposited nitride for the electrical point contacts; the third etch defines the metal contacts; the fourth etch creates a trench deeper than the first one in order to have a non (1 1 1) plane accessible to the anisotropic release etch; and the fifth etch releases the cell. Note that only 25 μm of material of the original

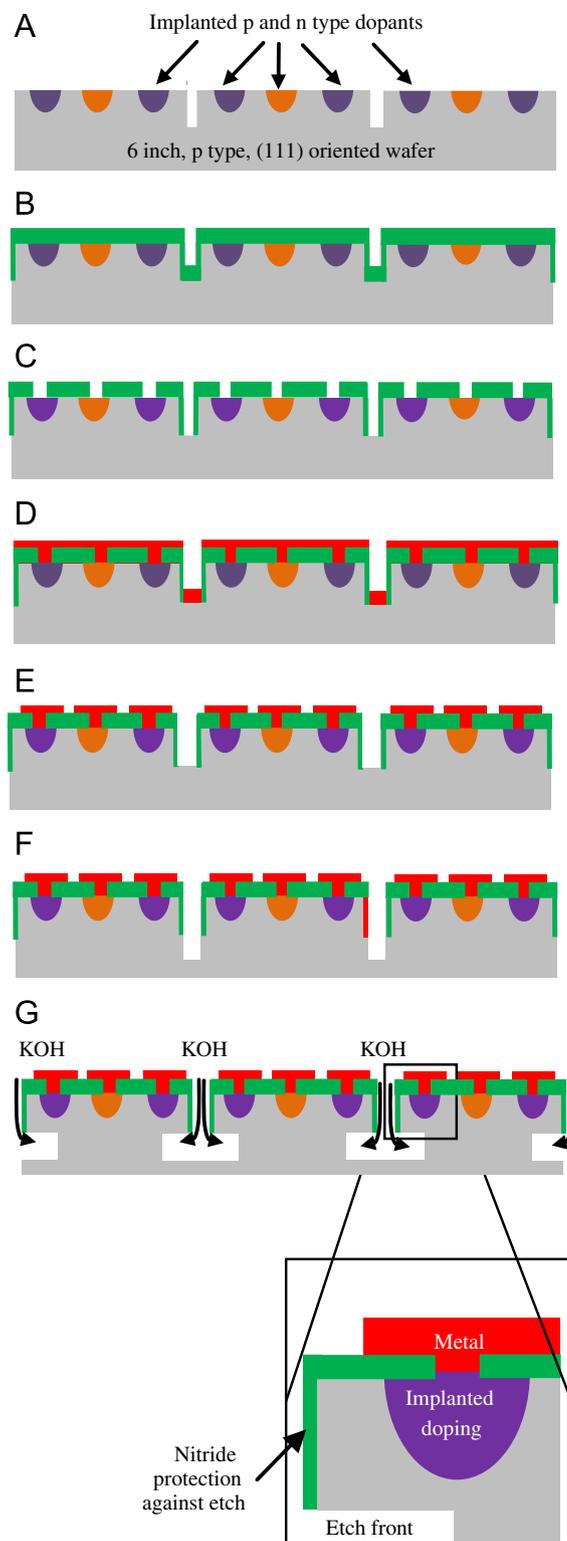


Fig. 5. Cross section illustrating the process flow for the creation and release of the cell: (A) First etch defines the size of the cell, (B) Low pressure CVD nitride deposition, (C) Second etch creates point contacts, (D) Tungsten CVD metal deposition, (E) Third etch patterns metal, (F) Fourth etch creates an etch front and (G) Fifth etch releases the cell.

wafer is consumed in the creation of the cells, leaving 675 μm of silicon for subsequent releases.

The first etch is performed by deep reactive ion etch (DRIE) or “Bosch process” targeted at an etch depth of 20 μm using SF₆ as

the etchant and a 2.2 μm thick, photolithography patterned photoresist as a mask. The nitride layer deposited between the first and second etch is done by low-pressure chemical vapor deposition (LPCVD). This layer is conformal and has a thickness of 1 μm ; the objective of this film is to protect the walls of the cell from the wet chemistry during the fifth etch. The second etch is done by reactive ion etch through a 1.8 μm thick patterned photoresist mask. A PECVD metallization step between the second and third etch is carried out by depositing low stress tungsten with a thickness of 200 nm. The third etch defines the interdigitated metallization pattern on the cell. The fourth etch is again with DRIE through a 1.8 μm thick patterned photoresist mask targeted to 25 μm depth.

After tungsten metallization and the creation of the 25 μm deep trench, the fifth etch is done. For this step, the wafer is submerged in a potassium hydroxide (KOH) 6 M solution held at 85 $^{\circ}\text{C}$ for 3 h and 45 min and left 24 h more at room temperature to detach the cells from the wafers. The solution accesses the unprotected silicon through the channels formed during the third etch. The nitride walls protected the material enclosed by them. Also, due to the orientation dependent etch rates, the (1 1 1) planes (parallel to the surface of the wafer) were etched very slowly. The averaged experimental etch rate selectivity between the (1 1 1) and (1 0 0) planes was 1:19, making the finalized cells

thinner than the designed thickness: around 13.7 μm instead of 20 μm . Fig. 6 shows images of attached and released cells.

3.2. Experimental optimization of cell passivation

Simulation results showed the importance of surface passivation. This is noteworthy because the released cells have a bare silicon front, resulting in a highly-reflective surface with high surface recombination. The high rate of surface recombination brings down the effective lifetime of the carriers and, with it, the overall efficiency. In order to increase the effective lifetime, a passivation layer needs to be introduced. Furthermore, an anti-reflection coating is required to increase light transmittance into the cell.

Alumina has been used successfully as a passivation layer on silicon substrates. It is desirable because it is deposited at temperatures below 200 $^{\circ}\text{C}$ [22,23]. Thus a passivation study of the cells was performed using atomic layer deposited (ALD) alumina in a custom designed viscous flow reactor. The obtained films were 79 nm thick and the growth temperature was 190 $^{\circ}\text{C}$. The best cells passivated with this layer produced a cell with 2.95% efficiency for samples annealed at 430 $^{\circ}\text{C}$ for 30 min on a hot plate and a cell with 4.14% efficiency for a sample annealed at 430 $^{\circ}\text{C}$ for 30 min in an oven with forming gas atmosphere.

Alternatively, silicon nitride layers rich in hydrogen have also been extensively used in photovoltaics for passivation. The literature explains [24,25] that hydrogen from the gas mixture is trapped in the nitride layer (in the form of Si-H and N-H bonds) during the nitride deposition and then released during the anneal steps. The hydrogen passivates dangling bonds on the silicon surface as well as in bulk defects. This makes these sites unable to attract and trap carriers thereby lowering recombination rates. Studies found in the literature for the optimization of this layer have been carried out in 10–15 times thicker substrates.

A two part process was designed to maximize the passivation performance of plasma enhanced chemical vapor deposition (PECVD) silicon nitride (Si_3N_4). The two processes explored in this optimization were (1) growth conditions and (2) anneal conditions. For the first part, we performed a full factorial experiment to maximize the passivation by studying three main variables [26] temperature (high or low), the RF power (high or low), and the concentration of the ammonia in chamber (high or low). High temperature condition was 350 $^{\circ}\text{C}$ for the top temperature of the chamber and 200 $^{\circ}\text{C}$ for the bottom. Low temperature condition was 150 $^{\circ}\text{C}$ for the top temperature of the chamber and 100 $^{\circ}\text{C}$ for the bottom. High RF power was 80 W and low RF power was 20 W. The high ratio between the ammonia (NH_3) and silane (SiH_4) flows was 1.25, while the low ammonia ratio was 0.25. Other variables were kept constant with pressure=900 mTorr, silane flow=200 sccm, helium flow=500 sccm, and nitrogen flow=300 sccm. The nitride thickness was targeted between 64 and 74 nm to produce the desired anti-reflection properties.

The open circuit voltage (V_{oc}) of 22 cells divided in 8 groups was used as a relative measurement of the passivation quality [27]. Fig. 7 reveals that the most influential parameter in this experiment was the deposition temperature. For all cases, higher temperatures produced higher average V_{oc} . For high temperature runs, a high RF power affected positively the V_{oc} of the samples. For the high temperature and high RF, the ammonia content had a small effect on V_{oc} . We opted to use the high temperature, high ammonia, and high RF power recipe to perform the anneal optimization because we obtained higher deposition rates and an index of diffraction closer to 2 (better AR coating for air-silicon interfaces). In addition, other researchers [28] have found better passivation properties with higher ammonia concentrations.

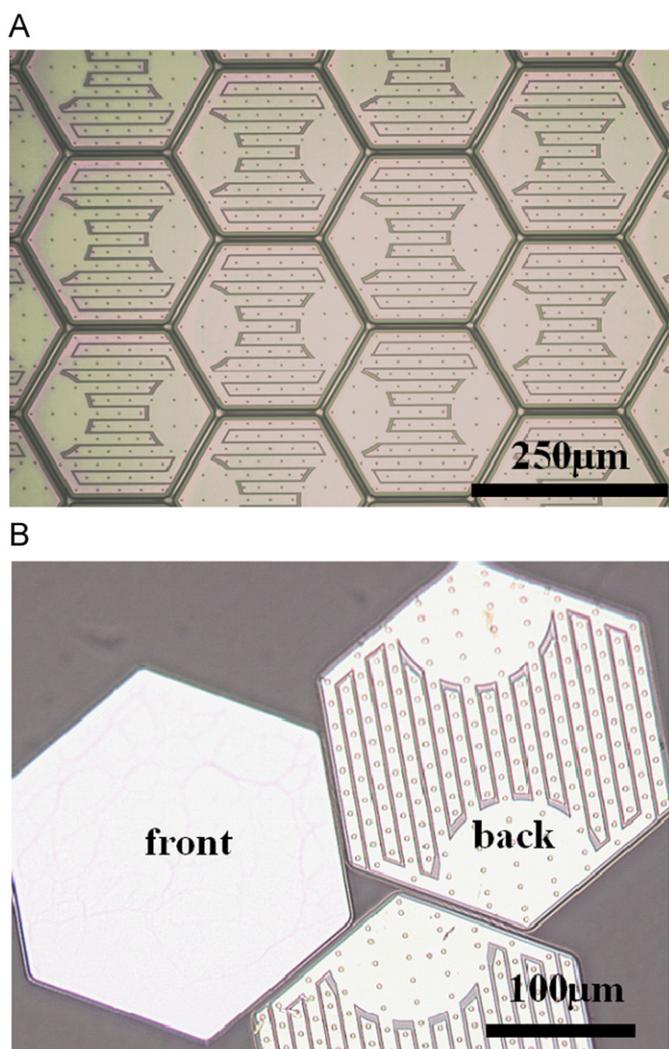


Fig. 6. Images of cells: (A) Array of 250 μm cells attached to the wafer (B) front and back of released cells.

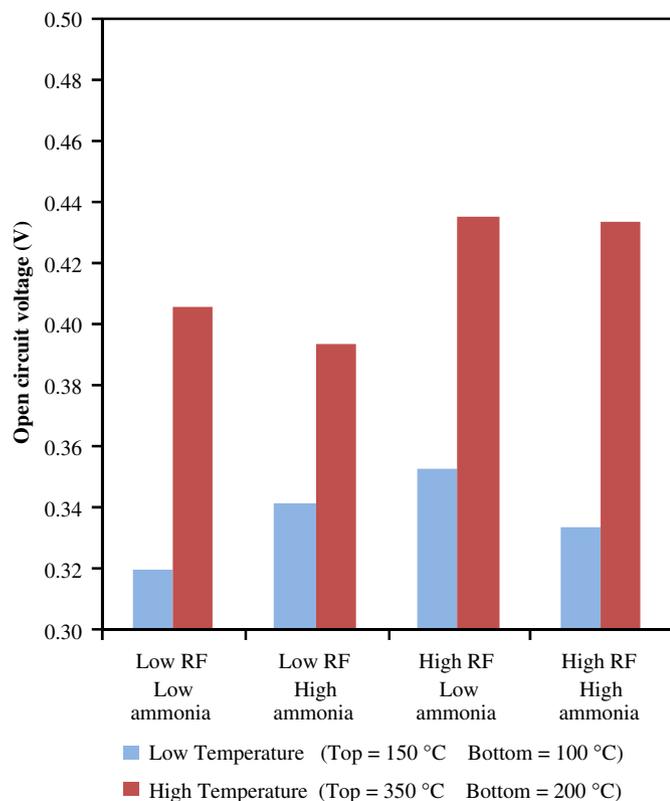


Fig. 7. Average open circuit voltage of the solar cells passivated with nitride for different processing conditions.

The second part of the experiment involved the optimization of the film annealing time. 70 nm of silicon nitride ($RI=1.9622$) were deposited using the best recipe (high temperature, high ammonia, and high RF power) from the first experiment in five sets of samples. This thickness and refractive index created a quarter wavelength coating optimized to transmit into the cell almost 100% of the light in wavelengths around 550 nm. A 450 °C forming gas anneal was performed in an EVG-520 wafer bonder oven. For the experiment, 4 sets of samples (each one is a glass slide with several micro cells on it) started inside the anneal oven in forming gas (3% H_2 , 97% N_2) at room temperature. All the cells for each slide underwent the same conditions. Once the temperature reached 450 °C, a slide was taken out at 1 h intervals, providing four different anneal times. A fifth set without anneal was used as a comparison at 0 h.

Fig. 8 shows the open circuit voltage obtained from the solar cells passivated under different anneal times. For increasing anneal time at 450 °C, higher voltages were obtained, peaking at 3 h and dropping after that.

3.3. Electrical and thickness characterization

In order to calculate the total thickness of the cells, a total of 17 cells were measured with an optical profilometer. On average, the measured thickness was 13.68 μm with a standard deviation of 0.379 μm . The span of thicknesses for all 17 cells ranged from 12.91 to 14.3 μm .

To make contact with the solar cells, a micro-dispensing unit and a MikrosPEN from EFD were used to dispense small amounts of silver paste onto the pads of the cell and create a bigger contact to extract the current. JV curves were obtained under 1 sun illumination conditions. A Spectrolab model XT-10 class A solar simulator

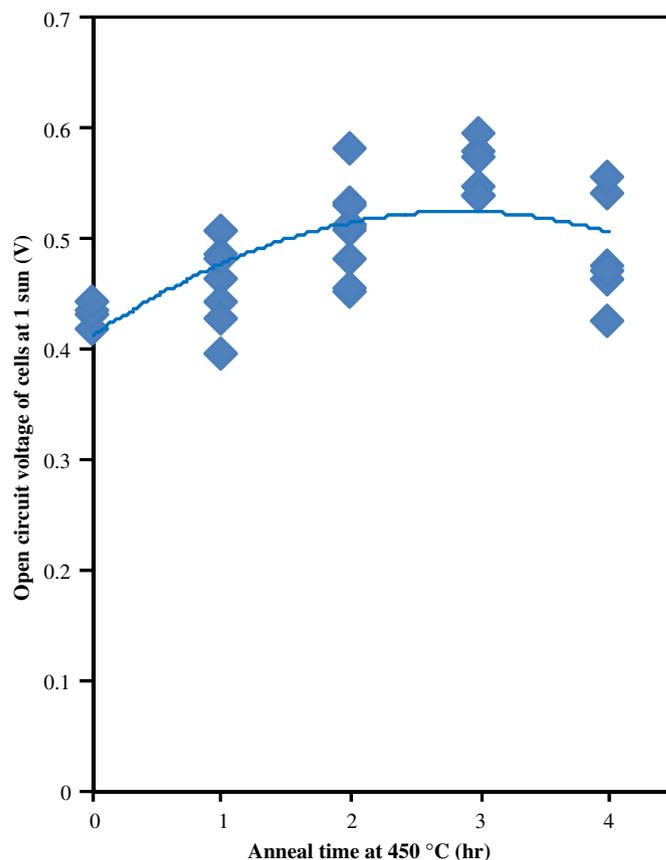


Fig. 8. Open circuit voltages for different annealing times. The diamonds represent the experimental data and the line a quadratic fitting.

with a 1 kW, short arc, xenon lamp was used for testing. The spectrum was normalized to 1000 W/m^2 using a silicon reference cell. The beam is an 88 inch² and the chuck is temperature controlled using thermoelectrics. The solar cell was connected to a Keithley model 4200 system with 4210 modules, with output sent to LabVIEW to be analyzed with internally developed software. The pads were then contacted by probes using the 4 wire method (force-sense) to reduce the effects of the resistance of the cables and connectors to do 1 sun calibrated measurements. The cells were measured in a pseudo-bifacial mode. Some reflected light from the chuck went back into the cell through the non-metalized area (13% of the total area of the cell). An average relative efficiency loss of 7.65% was observed when using a non-reflective chuck compared with a reflective chuck, given that we can expect close to 100% metal coverage on the back side of the cell in future iterations of the cell design.

Fig. 9 shows the result from the best cells with different passivation approaches for cells of identical junction/contact designs. The results were grouped in 4 categories: unpassivated, alumina coated, Si_3N_4 coated with no anneal, and Si_3N_4 coated with anneal. The legend describes the treatments applied to the cell as well as the efficiencies obtained for each curve of Fig. 9. The unpassivated cell is the one closest to the origin and with the lowest efficiency of 1.24% (gray dot). Besides having a low V_{oc} and current density (J_{sc}), it has a low fill factor. All of these attributes could be due to excessive recombination. The two subsequent curves (orange dot and dash) were treated with alumina. They show that the J_{sc} in the device has increased by a factor of two; however, the fill factor is still poor. The curves treated with Si_3N_4 without anneal (blue dot and dash) show increased efficiency due

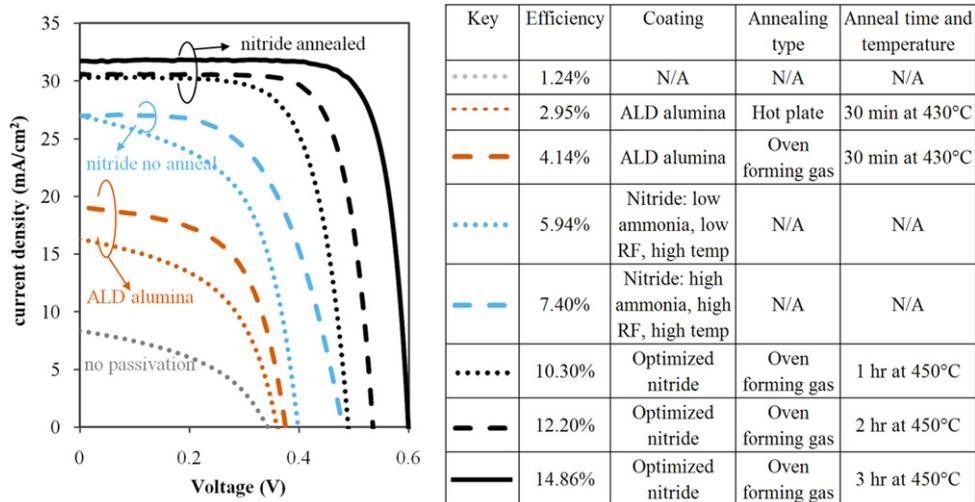


Fig. 9. Best J - V curves of micro cells with different passivation schemes. The highest efficiency curve (solid black) corresponds to a cell with a current density of 31.75 mA/cm^2 , a fill factor of 78.4%, a V_{oc} of 597 mV, and an efficiency of 14.86%.

to improved V_{oc} and J_{sc} . However, the fill factor was not improved. It was not until the forming gas anneal together with the optimized nitride was introduced that the fill factor of the curves was improved significantly. Between the three curves with nitride and anneal, the fill factor is quite similar, but the short circuit current density and particularly the open circuit voltage improves as the anneal time is increased.

Recalling the simulation results from Fig. 4, it was seen that the lower the SRV number, the higher the efficiency obtained. Alternatively in Fig. 9, it was seen that certain films and anneals applied to the cell lead to higher efficiencies than others. It is important to note that the only difference between the cells was the passivation process of the thin layers applied. Thus, it can be inferred that the higher efficiencies obtained during the optimization steps were due to a lower SRV (higher passivation quality). Finally, by comparing the highest efficiency J - V curves of both simulated and experimental results, it can be concluded that the SRV in our best fabricated cell is below 100 cm/s .

4. Conclusions

Tools and technology from the microsystems arena were used to simulate, design, fabricate, and release small form-factor solar cells that are 10–15 times thinner than typical commercial crystalline silicon cells. Surface passivation is crucial in these thin and small devices. Simulations showed that depending on the quality of the passivation a $14 \mu\text{m}$ thick back contacted device with point contacts could have efficiencies ranging from 1% to 15%. In our experiments, passivation with a silicon nitride layer was found to be superior to ALD alumina. Finally, a $14 \mu\text{m}$ thick, $250 \mu\text{m}$ wide photovoltaic cell was created and optimally passivated to yield 14.9% efficiency.

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